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FINAL REPORT

Development of Multilayer Epitaxy for High Reliability Transistors

July 1966 through March 1967

Contract No. NAS8-18125
DCN 1-6-40-68627 (1F)

National Aeronautics and Space Administration
George C. Marshall Space Flight Center
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ABSTRACT

This report describes design and process technology employed to develop multi-layer epitaxy for high reliability transistors. All of the devices generated were NPN transistors with epitaxially grown collector and base regions and diffused emitters. In order to determine the effect of various base widths and resistivities on switching speed and peak power capability, transistors rated at 30 amperes were designed, fabricated, and evaluated. The resulting information was used to establish conditions for the 100-ampere final samples. The epitaxial techniques employed yielded essentially defect-free material which is a requisite for large area, high power transistors.

X-ray diffraction topographic studies were made to check the material perfection and to improve the processing.

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I. INTRODUCTION

This report will describe the research and development conducted by the Westinghouse Electric Corporation, Semiconductor Division, Youngwood, Pa., and the Research and Development Center, Pittsburgh, Pa., to develop silicon power transistors with lower saturation resistance and with improved and higher rating on second breakdown voltage and frequency response. This study was initiated in July 1966 for National Aeronautics and Space Administration, G. C. Marshall Space Flight Center, Huntsville, Ala., under Contract NAS8-18125.

One objective was to reveal the secondary breakdown characteristics of a large area single chip, multi-layer epitaxial 100-ampere, 150-volt transistor. The base thickness and active region doping profiles were the major parameters under investigation for optimization of frequency and secondary breakdown performance.

A. DEVELOPMENTAL SEQUENCE

In order to obtain an adequate number of samples of several different base widths and resistivity profiles, it was decided that the 30-ampere epitaxial transistor be used as a test vehicle. The geometry and package configurations of this device are detailed elsewhere in this report. Although the encapsulation techniques differ, it is felt that the electrical results, particularly peak power or secondary breakdown and frequency response, can be correlated directly.

Design calculations were acquired, with the aid of a computer program, for three ranges of base widths: 2-4 microns, 10-12 microns, and 18-20 microns. Resistivity profiles for both punch-through and avalanche breakdown were obtained for all three groups. Thirty-ampere samples were processed

accordingly and their electrical characteristics were evaluated. On the basis of the results obtained, the parameters were established for two sets of 100-ampere final samples.

B. MAJOR ACCOMPLISHMENTS

One of the major problems associated with large area devices is that of maintaining junction uniformity and material homogeneity. This problem was solved by carefully controlled epitaxial growth techniques and diffusion processes. A joint effort by the Power Device group of the Westinghouse Research and Development Center and the Westinghouse Semiconductor Engineering group provided revealing information through the use of X-ray topography to display crystal defects. As expected, the epitaxial layers were relatively defect-free; however, strains were induced during subsequent processing which may or may not have influenced device performance. Processing changes were made in an attempt to reduce the incidences of defects. One such change was to support the wafers horizontally on a quartz boat instead of standing them in a slotted quartz boat during diffusion. This significantly reduced the number of detected defects.

Test sets were designed and constructed to provide the capability of measuring switching times at collector currents of 75 amperes and to determine the frequency response of the subject devices.

Correlation was established for base width, frequency response and secondary breakdown; the compromises were resolved and devices were fabricated to the optimized parameters.

II. DESIGN CONSIDERATION

The main purpose of this contract is to fabricate high power (V_{CEO} = 150V and I_C = 100A) devices with good secondary breakdown protection. The discussion in this section will, therefore, be mainly confined to secondary breakdown phenomenon.

A. SECONDARY BREAKDOWN

From the point of view of device design, there are three fundamental ways in which the breakdown of the collector-emitter voltage takes place: 1) avalanche mode; 2) punch-through mode; and 3) $\alpha M_o = 1$ mode. These were recognized very early in the development of high power transistors for high voltage capability.

The avalanche breakdown is empirically represented as

$$1 - \frac{1}{M(v)} = \int_o^w \alpha_i(E)\, dE \qquad (1)$$

where M(v) is the multiplication factor, w is the depletion layer width and $\alpha_i(E)$ the ionization rate. As the applied voltage of the collector junction increases, the field intensity also increases, which in turn increases the ionization rate. When the integral in (1) becomes unity, M(v) approaches infinity and the collector junction breaks down.

The punch-through voltage is defined as the voltage at which the collector depletion layer region reaches the emitter junction causing a dynamic short circuit to exist between emitter and collector. At punch-through, the injection efficiency and the transport factor are both equal to one and the current gain of the transistor is also equal to one.

The $\alpha M = 1$ breakdown can be understood by studying the V-I characteristic of a transistor. The collector current, I_C, is related to the saturation current, I_S, as

$$I_C = \frac{MI_S - I_B}{1 - \alpha M} \tag{2}$$

where I_B is the base current and α is the collector to emitter current transfer at the corresponding current level. When αM approaches one, I_C approaches infinity and a collector-emitter breakdown will occur. This is referred to as $\alpha M = 1$ breakdown. When the base current is absent, it is the same condition for determining the sustaining voltage, V_S, or V_{CEO}. The multiplication factor can be expressed empirically as:

$$M = \frac{1}{1 - (V/V_B)^{1/n}} \tag{3}$$

when $\alpha M = 1$, $V = V_{CE}$ and hence,

$$\frac{V_{CE}}{V_B} = (1 - \alpha)^{1/n} \simeq \left(\frac{1}{h_{FE}}\right)^{1/n} \tag{4}$$

where h_{FE} is the collector to base current transfer ratio and n is a constant (≈ 3 for silicon NPN transistor). Once the $\alpha M = 1$ breakdown voltage is reached, I_C will increase which in turn varies α. At lower current level, α increases with current. Since the condition that $\alpha M = 1$ is maintained, an increase in the value of α requires a lower value of the multiplication M. However, a decrease in M implies a reduction in voltage across the unit and a negative resistance region exists. The effect of the negative resistance can be minimized by controlling the variation of α over the operating current range.

It has been found that the V-I characteristic at high current levels shows a drastic decrease in the collector-emitter voltage. This phenomenon is called secondary breakdown, which is especially pronounced in high speed or high frequency transistors with high gain. In recent years with the increasing number of power transistor manufacturers, this was generally christened as secondary breakdown. Often when the operation of the device enters into any of these conditions, this type of secondary breakdown destroys the unit.

It was widely recognized through various investigations that junction uniformity is extremely important. If a local area has higher current density, thus generating a hot spot, it can cause a large proportion of the current to flow into this area while the rest of the junction serves as a reservoir due to junction capacitance. This can appear as a constant voltage trace on the scope and at the same time can cause the local area to reach an extremely high temperature, approaching the melting point of the materials. Transistors with narrow base widths are highly susceptible to this phenomenon, due probably to the exaggerated effects of pipes and/or dimples resulting from material or processing induced defects.

B. CURRENT GAIN

For transistors with fairly narrow base width, the transport factor is close to unity; and, hence, the factor that influences most of the current gain is the injection efficiency γ. In the case of diffused transistors, γ is mainly determined by surface concentrations, diffusion depths, lifetime of the minority carriers and the drift field intensity. The dependence of γ of these parameters can be determined by solving the steady state continuity equation for known boundary conditions. This analysis has been done at Westinghouse using a computer program. The program computes the injection efficiency, the transport factor and current transfer ratio for given values of surface concentrations, diffusion length and junction depths, also taking into consideration the effect due to drift field. At low-level injection, the drift field is due to the built-in concentration gradient; and at high level, the drift field is mainly due to the injected carriers.

In general, emitter efficiency and current gain tend to increase with emitter current as recombination consumes less of the injected current and to decrease at high current levels due to an effective increase of carrier concentration in the base (conductivity modulation). These effects combine to give a gain characteristic which is low at very low current, rises to a maximum at moderate currents, and falls off at high currents. Gain at very high current is determined largely by emitter edge length, since the transverse voltage drop across the base region leads to crowding of current to the emitter edges. For the best utilization of total device area at high currents, the ratio of emitter edge length to emitter area must be reasonably large. Theory and experience both indicate that the current density per unit of emitter edge length should be on the order of 4-5 amperes per inch. Thus, the subject 100-ampere transistor requires some 20-25 inches of emitter edge.

The control of gain at low and moderate currents can be achieved by a suitable design of the overall emitter area and of the emitter doping level. By increasing the total emitter area, recombination is made a dominant factor up to higher emitter currents; in this way, the peak of the gain curve is lowered in magnitude and shifted to higher current levels. The gain fall-off is thus reduced and saturation voltage is also minimized. The total emitter area should therefore be as large as physical limitations and switching time considerations permit.

The fundamental emitter efficiency can be controlled by the emitter doping level or, in the case of a diffused emitter, by the relative depth of diffusion and the surface concentration, as is well known to the industry. In the subject device, the emitter efficiency is controlled to the lowest level compatible with gain requirements; i.e., the doping level in the emitter is high enough to achieve the desired gain, but no higher. In the case when base width is wider the transport factor β does lower the gain due to excessive recombination. The upper limit of base width within the 2-20μ range is therefore governed by the gain requirement.

C. DESIGN DETAILS

The subject transistor employs the same emitter geometry as the 100-ampere transistor fabricated for NASA Contract NAS8-5335. The design consists of 45 emitter fingers with a total emitter edge length equal to 21 inches and a total emitter contact area equal to 0.5 $(in.)^2$. The detailed dimensions of the design are shown in Figure 1.

The impurity profile is a double-epitaxial, single-diffused profile. The collector and base regions are grown epitaxially and the emitter is formed by diffusion. The profile of such a structure is shown in Figure 2.

Detailed design calculations were performed at Westinghouse to establish the dependence of breakdown voltage and avalanche multiplication factor on device parameters. The results of a set of calculations are shown in Figure 3. This figure gives the punch-through voltage and avalanche voltage as a function of base width, W_B, and background concentration, C_B. It also shows the breakdown voltage for M = 2, M = 1.1 and M = 1.05. The curve for $M = \alpha$ corresponds to avalanche breakdown.

Designs were calculated for several groups of devices with base widths in the range of 2 to 15 microns and resistivity in the range of 0.1 to 10 ohm-cm. The parameters used for a typical group are:

Emitter surface concentration	$C_1 = 1 \times 10^{21}$ atoms/cm^3
Base doping	$C_2 = 1 \times 10^{18}$ atoms/cm^3
Emitter depth	2.5μ
Base width	2.5μ
Collector thickness	18μ

The measured and the calculated values of the breakdown voltage of this group of transistors are shown in Figure 4. Additional electrical results are discussed in detail in Section VI.

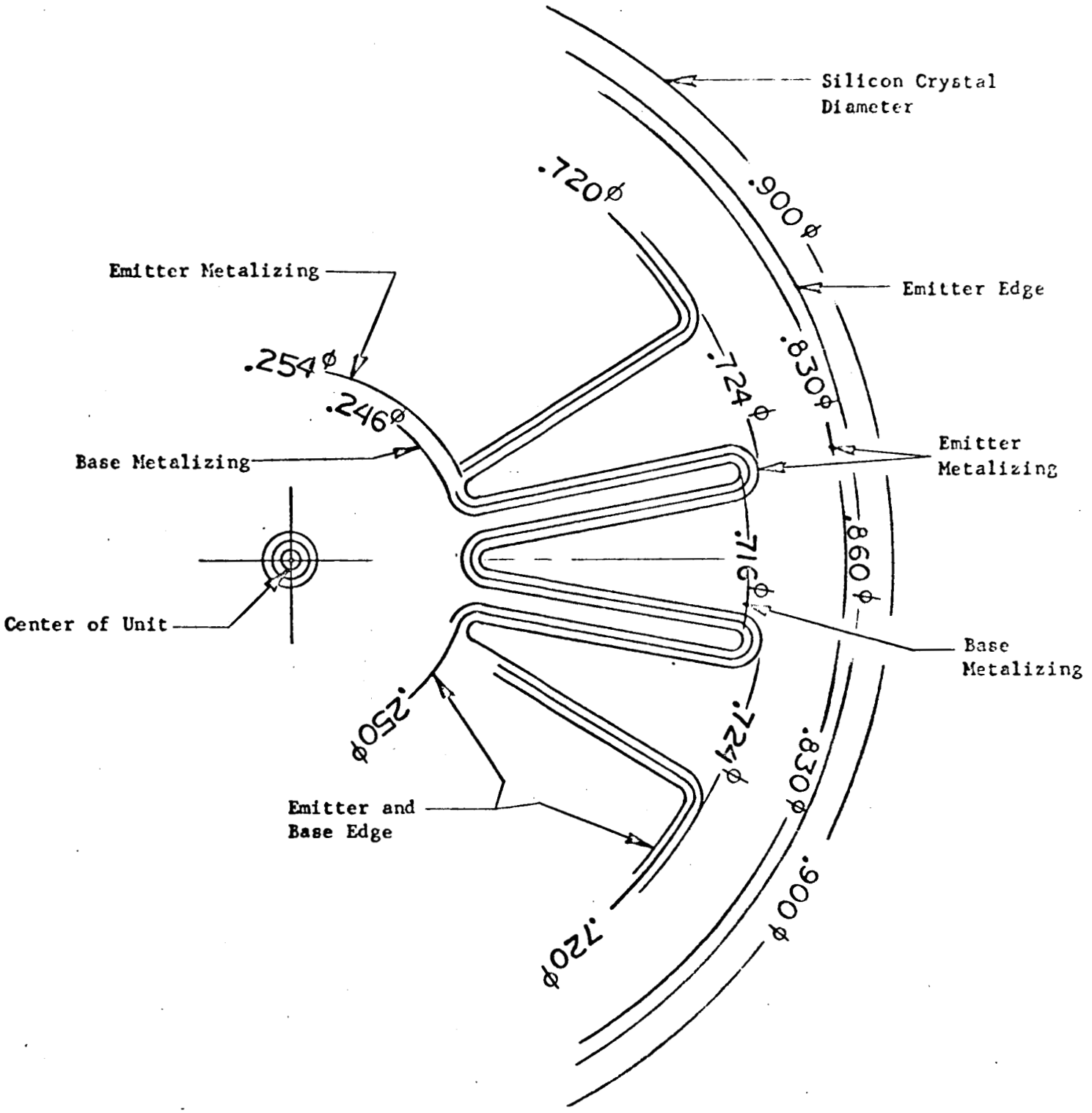


Figure 1: 100-Amp Transistor Final Design

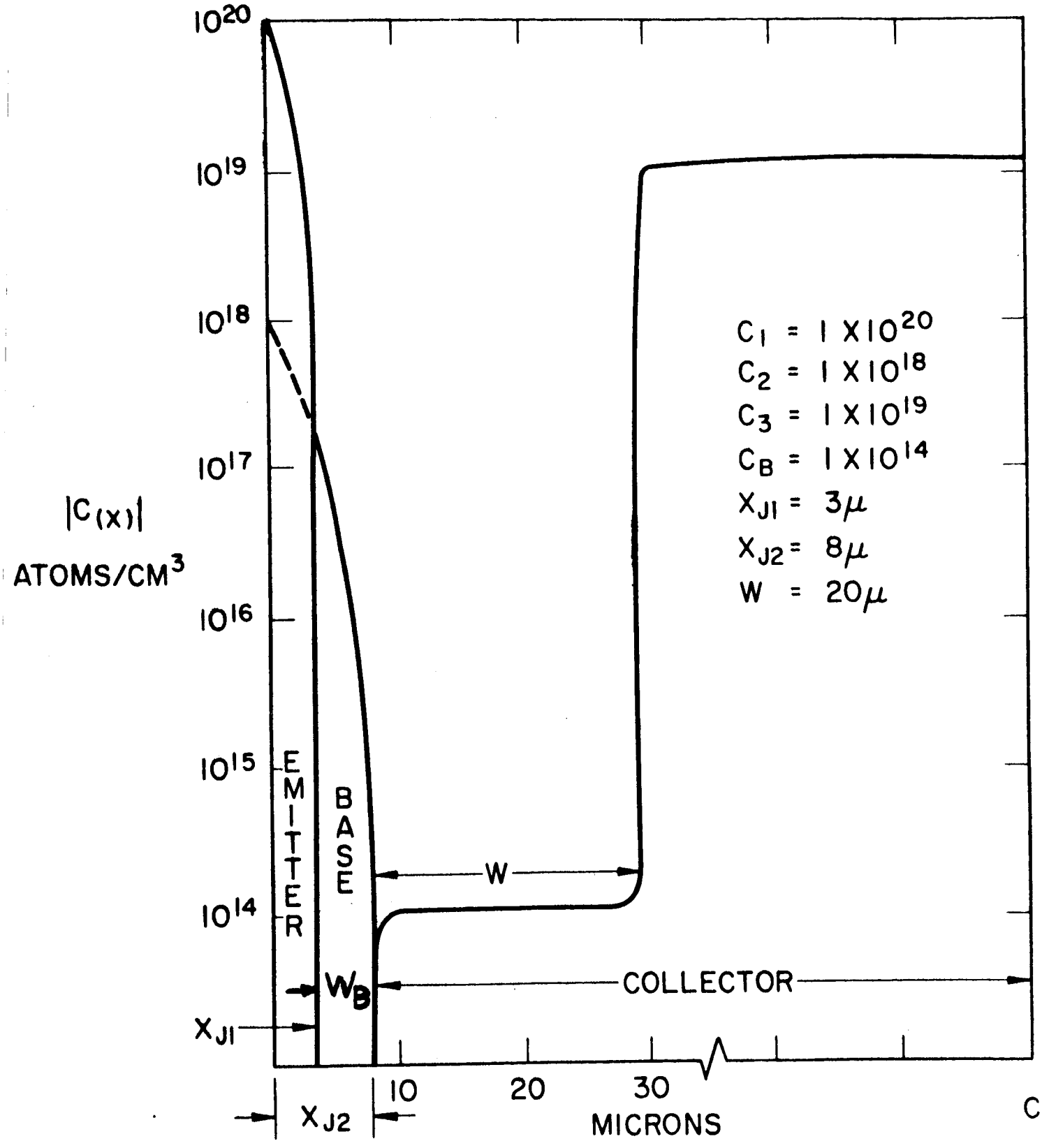


Figure 2: Impurity Distribution of Double-Epitaxial Transistor

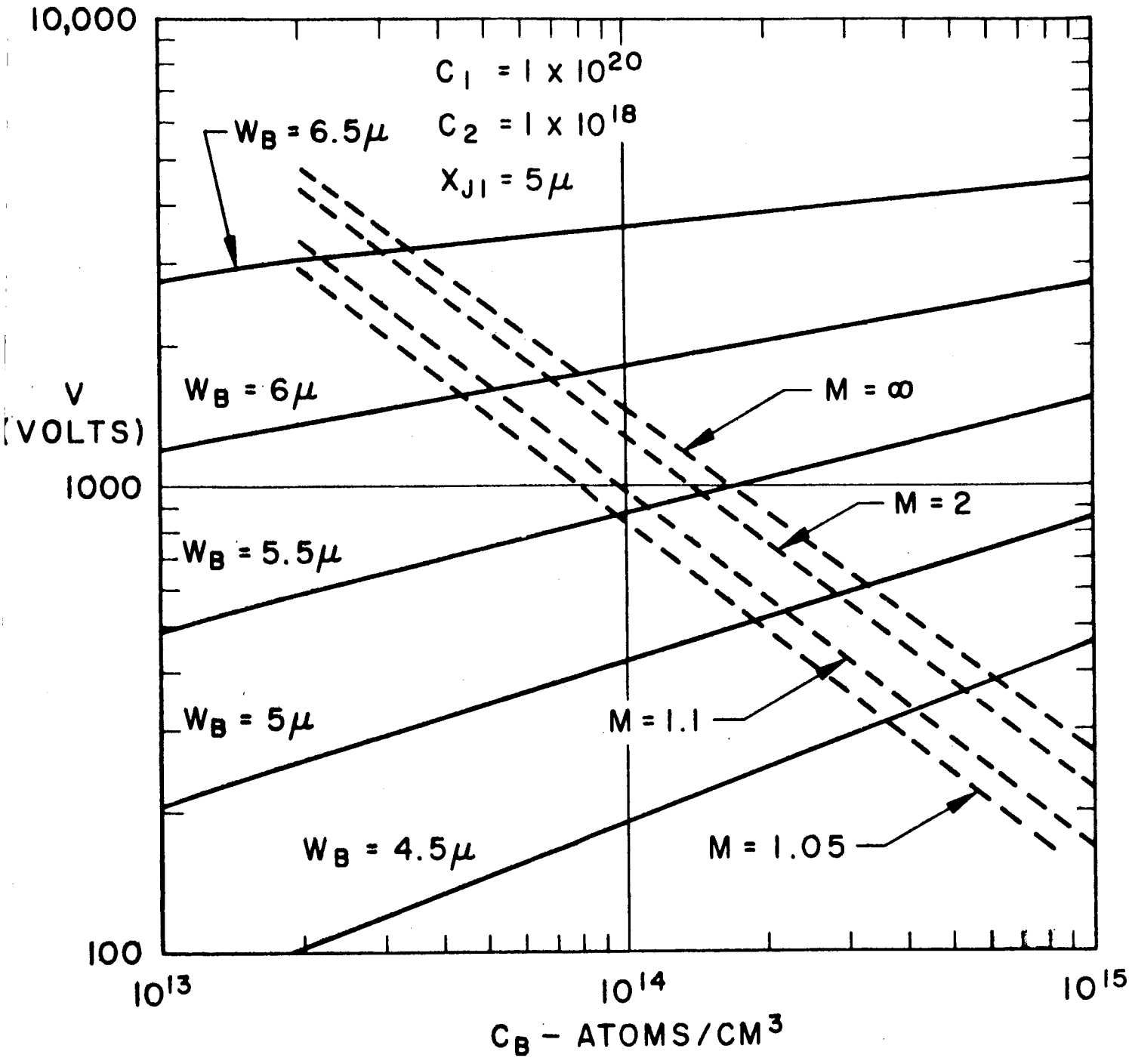


Figure 3: Breakdown Voltage Design Calculations

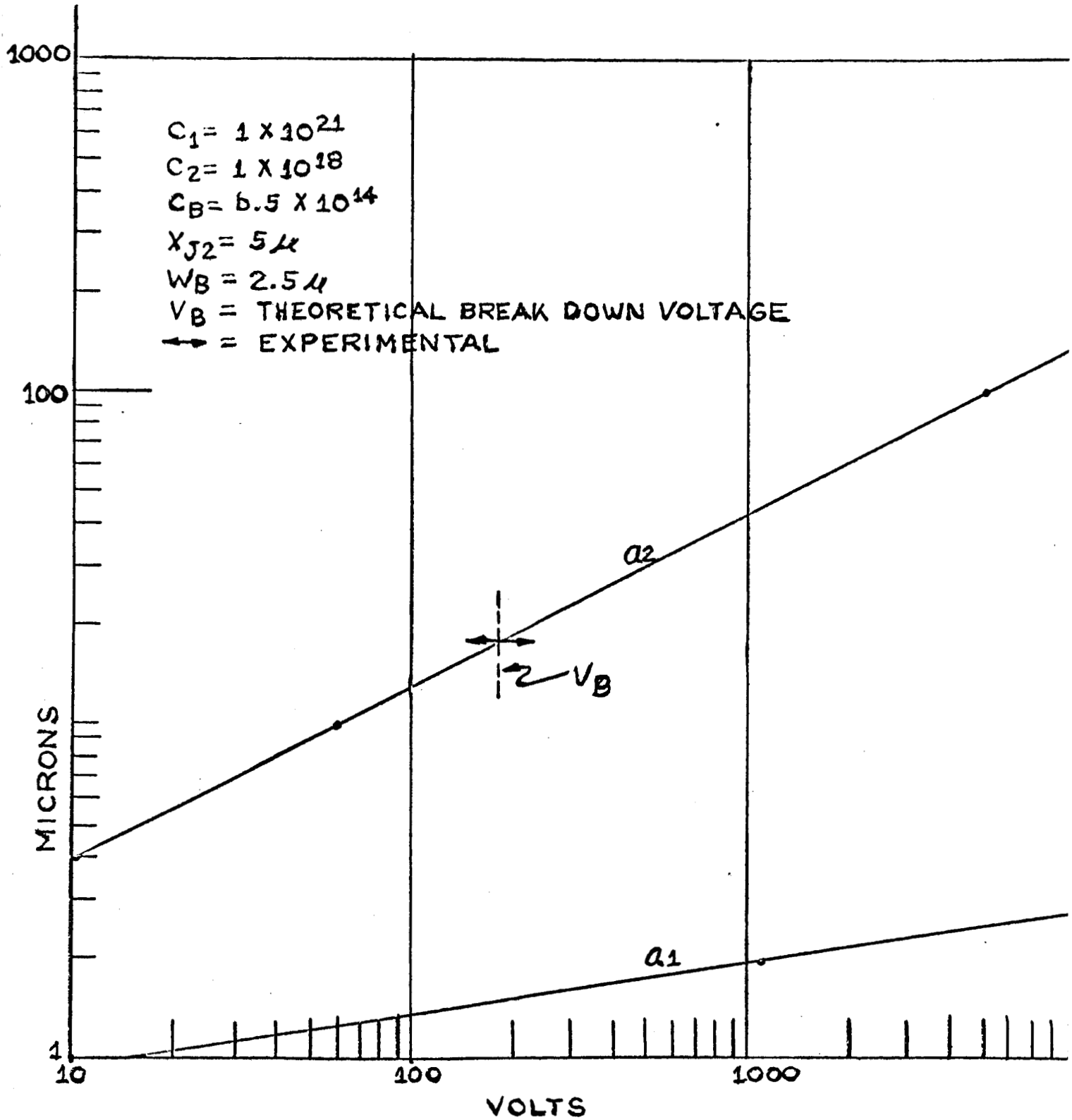


Figure 4: Breakdown Voltage vs. Base Width

III. MATERIAL PREPARATION

A. BACKGROUND - EPITAXIAL DESIGN

The present method for producing silicon epitaxial overgrowth on silicon involves a crystallization from the gaseous phase by the aid of the chemical reaction between silicon tetrachloride and hydrogen at elevated temperatures. Similar such processes have been used for the past 100 years for the production of crystals.

The substrate on which oriented crystallization of a single crystal layer takes place need not consist of a crystal identical to the crystallizing substance. This follows from numerous facts concerning epitaxial overgrowth to which many investigations have been devoted since Frankenheim's[4] time. It is sufficient for the lattice of the substrate to possess the necessary metric and energy compatibility with the crystallizing substance or even for its surface to be compatible in metric and energy respects with at least one principal force of the crystallizing substance. The kinetics and regularities of such growth were thoroughly studied by Dankov[5] who formulated the principle of crystallographic correspondence.

The first stage in crystal growth from the vapor phase must be the formation of a nucleus. This is the smallest number of atoms capable of sustaining further growth, units smaller than this tend to evaporate. This requires molecules to condense into clusters and grow until a critical size has been passed. Clearly, if the pressure of the molecules is very high, i.e., if the vapor is supersaturated, then there will be increased tendency for the molecules to condense into clusters and grow into nuclei. The supersaturation required for growth of a nucleus may be very high; indeed, it can be shown supersaturations of about 50% may be necessary. Supersaturation is usually defined as α where

$$\alpha = \frac{\rho}{\rho_o} - 1$$

(4) L. M. Frankenheim, Poggend. Ann., 37,516 (1936).
(5) P. D. Dankov, "Proc. of the Second Conf. on the Corrosion of Metals," 2, 120 (1943).

ρ = pressure of vapor

ρ_o = equilibrium vapor pressure of the condensed phase at that temperature.

Once formed, the nucleus begins to grow. Atoms from the vapor collide with the nucleus, diffuse over the surface until they either find a suitable site or fly off into the vapor again. Atoms condensing on the surface lose latent heat causing the surface to be at a higher temperature than the bulk of the crystal. Surface temperatures 100°C higher than the bulk temperature have been suggested by Wilman[6] as a factor contributing to the mobility of atoms on the surface.

Atoms condensing on the surface will prefer sites with a maximum number of nearest neighbors because at such sites the bonding energy is at a maximum. Occupation of such sites would produce close packed surfaces over the nucleus. At this point, further condensation becomes difficult. For further growth, sufficient atoms must come together to form an island "nucleus" on the close packed surface. Once formed, the island may grow laterally to the extremities of the surface and then for further growth another nucleus must be formed. This process is similar to the formation of the original nucleus.

The concept of growth by two dimensional nucleation has been considered by several workers and it is possible to estimate the rate of nucleation; i.e., the rate of formation on monolayer islands and also to estimate the degree of supersaturation required to cause detectable growth. The theoretical value of the latter is of the order of 25 to 50%. However, in practice, it has been found that crystals may grow at low supersaturation of about 1%. This anomaly was explained by Frank[7] who proposed the mechanism of crystal growth which follows. He pointed out that if atoms are added onto the steps of a screw dislocation, a close packed surface of the type described in the previous paragraph was never formed but instead a growth spiral resulted. It should be realized that the origin of

(6) H. Wilman, "Proc. Phys. Soc.," London, 1368, 474 (1955).
(7) F. C. Frank, "Disc. Faraday Soc.," No. 5, 48 (1949).

dislocations and growth spirals is not completely understood. They may be created in the nucleus by thermal agitation or mechanical deformation or introduced during subsequent development of the nucleus. This suggests that the dislocation density can be reduced if conditions during growth are made as free from fluctuations (thermal and mechanical) as possible.

Since the substrate acts as an initial "nucleus" in epitaxial overgrowth, it must be expected that the perfection of overgrowth would depend upon the crystallographic orientation of the substrate. This has been observed in germanium where it was found that the rate of germanium overgrowth was dependent on the substrate crystal orientation for the most densely packed faces <110>, <111>, and <100>. Owing to the strong bonding forces acting in the planes of these faces, condensing atoms will be oriented in the correct way.

The perfection of overgrowth also depends on the temperature of the substrate. It has been found that silicon overgrowths prepared at a substrate temperature of 1270°C show a high order of perfection while the overgrowths prepared at 1175°C are less perfect. These results suggest that during deposition, the high-surface mobility of silicon atoms attained at 1270°C is essential for good film perfection. The high-surface mobility of silicon atoms enables them to diffuse over the surface and to find correctly oriented positions.

A further requirement for the preparation of good epitaxial overgrowth is that the substrate must be free from surface defects. For example, in the case of silicon good epitaxial overgrowth cannot be obtained in the presence of a substrate surface oxide. The latter provides nucleation sites for polycrystalline growth.

In the epitaxial overgrowth of silicon, the deposited silicon is produced by the hydrogen reduction of halosilanes such as silicon tetrachloride, the reduction of which may be represented by the simple equation:

$$SiCl_4 + 2H_2 \rightleftharpoons Si + 4HCl.$$

This equation does not predict the observed yield of other chlorosilane compounds or the yield of high molecular weight polymers of the homologous series $(SiCl_2)_xH_2$, such as $Si_{10}Cl_{20}H_2$, found as a condensate on the reaction walls. To account for the reaction products, it is possible to formulate numerous equations which represent possible reaction mechanisms. The standard free energies for a few of these reactions have been calculated (See Table I), and it may be seen that all are thermodynamically possible. An investigation has been carried out to evaluate, by means of gas chromatography, the reaction products of the silicon tetrachloride and hydrogen reaction.

It has been found that the epitaxial overgrowth rate of silicon is effected by the hydrogen to silicon tetrachloride molar ratio and also the hydrogen flow rate. The causes for these effects are not understood completely. It has been suggested that owing to the relatively high activation energy found for the hydrogen-silicon tetrachloride reaction and reduction in growth rate found by increasing the molar ratio above 0.1 that the following mechanism is possible. First there is adsorption of a silicon subchloride, probably the free radical $SiCl_3$, on the substrate surface and this is followed by loss of chlorine by reaction with hydrogen. However, the occurrence of adsorption phenomena at high temperatures seems doubtful and until further work has been carried out, particularly on the identification of reaction products, the kinetics of the reaction of hydrogen with silicon tetrachloride will remain obscure.

B. REQUIREMENTS FOR EPITAXIAL GROWTH

The epitaxial surface requirements for the large area transistors are stringent; no defects are tolerable over the entire active region. Small area devices can tolerate several defects since these units can be discarded. However, the presence of one defect in a large area configuration would nullify the unit because of the resultant low voltage or short characteristics. It has been determined that all epitaxial defects originate at the substrate epitaxial layer interface and are dependent on surface cleanliness, substrate perfection and system purity.

TABLE I

Standard Free Energies for Typical Reactions

Reaction	Standard Free Energy for Reaction at 1533Å (1270°C)
$SiCl_4 + 2H_2 = Si + 4HCl$	-1.9 Kcal/mol
$SiCl_4 + Si = 2SiCl_2$	-2.2
$SiCl_2 + H_2 = Si + 2HCl$	-1.2

1. Substrates

The substrates used for the subject devices are degenerate in that they are heavily doped with impurities. The doping level of the substrate was selected to obtain the designed saturation voltage characteristics. Heavily doped substrates inherently contain sufficient impurities to distort the crystal lattice. Distortions caused by precipitates or inclusions will not permit a sufficiently good lattice match for defect-free epitaxial growth. These distortions can be eliminated by careful selection of the parent crystal growth conditions and the type of dopant. Evaluation of the substrate material is accomplished by examination of the chemically polished surface prior to epitaxial growth. A chemically polished surface was employed for this device to insure a damage-free surface and to permit microscopic examination of the surface before growth was initiated.

2. Substrate Preparation

Preparation of the substrate material before epitaxial growth is a deciding factor in producing defect-free epitaxial layers. Heavy metal impurities, such as aluminum or iron, are retained by the substrate after the slicing and doping operations. These can give rise to foreign nucleation sites during the growth process. Wetting agents or solvents do not effectively remove these heavy metals. However, chemical techniques, such as reactive chloride acids, convert most heavy metals to water soluble metal chlorides and are easily removed by subsequent rinsing in deionized water.

3. Epitaxial System Purity

Epitaxial growth perfection is also dependent on system purity; that is, the environment in which the chemical reduction of the halide takes place.

a. Gas System -- The gases used in the epitaxial process must be of good quality. The hydrogen used for the reduction is passed through a Deoxo unit to remove traces of oxygen and then through a dryer to remove moisture to a level of less than 1ppm. All gases are filtered through submicron filters to remove foreign particles before they enter the reaction chamber.

The control of the gases, the valving and the piping required to mix and dilute are all done in a system that is leak proof. The materials of construction are Teflon and quartz to maintain gas purity prior to the reaction chamber.

b. Reactor -- A horizontal RF heated epitaxial system was used for all the transistor substrates (Figure 5). The susceptor was a pure grade of graphite coated with silicon carbide. The silicon carbide is deposited on the graphite under the same conditions required for epitaxial growth to insure a noncontaminating or defect contributing source.

The reactor tube was of quartz, and the susceptor is supported on a quartz sled. Reactor tube and susceptor loading is accomplished in a positive pressure hood to minimize dust or environmental particles from contaminating the surfaces of the slices.

c. Epitaxial Procedure -- The epitaxial procedure for the 30 and 100 amp device consists of heating the substrates to 1200°C in a filtered dry hydrogen atmosphere. Pure gaseous HCl is introduced to etch the substrates prior to growth. The reaction of HCl and silicon is the reverse of the deposition reaction and permits the removal of the environmental work damage caused by chemical polishing.

$$4HCl + Si \longrightarrow SiCl_4 + 2H_2$$

Sufficient silicon is removed to insure a lattice match for the growth operation.

The HCl procedure is followed with a pure hydrogen treatment at 1200°C to clean out the reaction area of any chlorides which could act as nucleation sites. A layer of N-type conductivity in the resistivity range of 8-12 ohm-cm is deposited to the required thickness. A P^+ layer is then deposited in situ to the desired thickness and the resistivity is controlled with diborane gas as the dopant. After the P^+ deposition, the system is purged with pure hydrogen to remove the dopant and halide traces. The system is then cooled for the removal of the substrates.

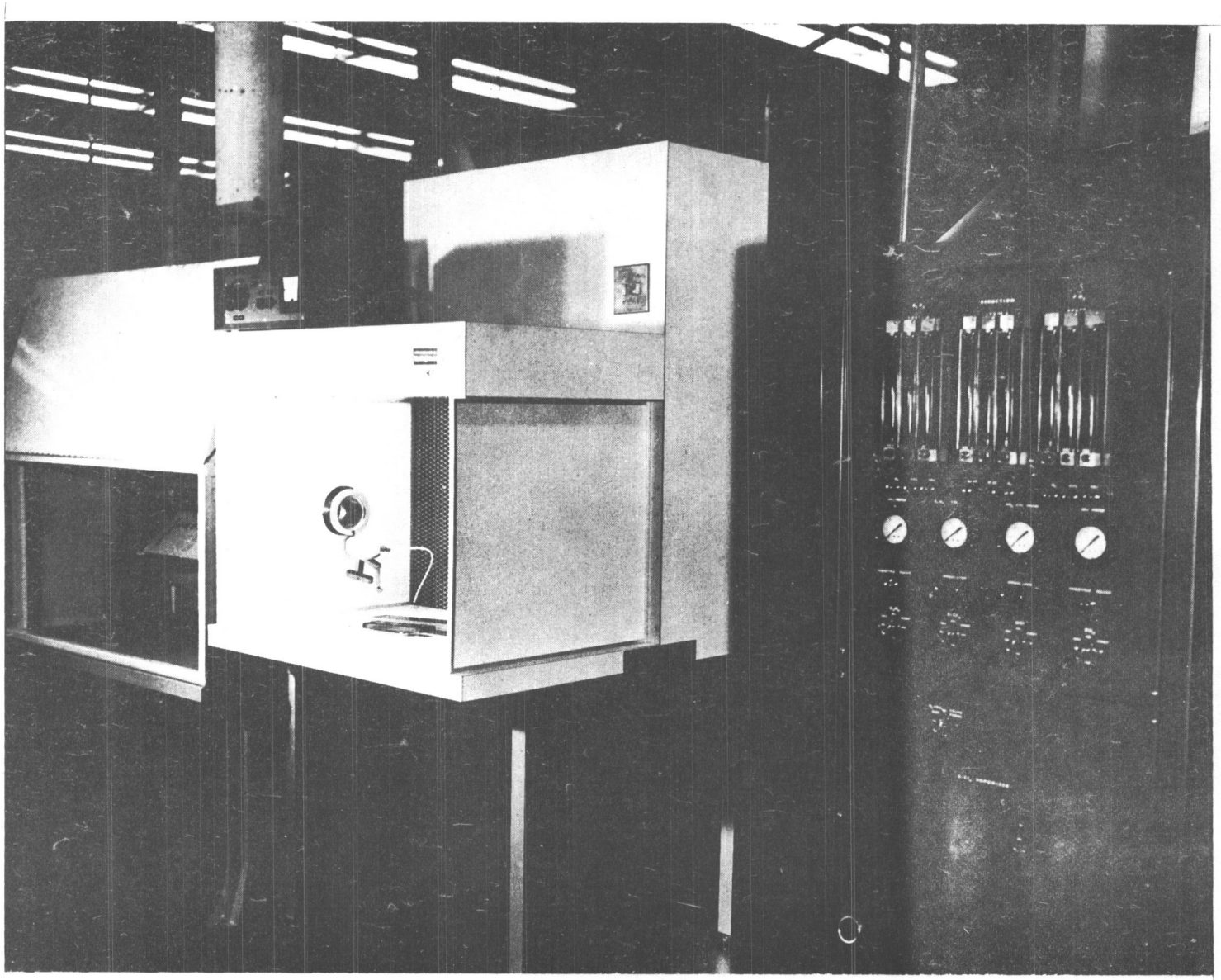


Figure 5: Epitaxial Furnace

C. MATERIAL REQUIREMENTS

Crystal Specifications:

N-type
Resistivity: .008-.01 ohm-cm
Radial resistivity gradient: 15% (Max.)
Diameter: 1.3" $\pm$ .001"
Dislocation density: 0-200/cm^2
Orientation: within 2° of the (111)
Lifetime: as high as possible
Lineage: None
Other imperfections: None

D. EVALUATION OF MATERIAL

1. Conductivity

This measurement determines the majority carriers in the silicon crystal. Two methods are employed at this laboratory -- thermoelectric cold probe method (See Figure 6) and the point contact rectifier method.

2. Resistivity

The resistivity is measured every inch down the length of each crystal to insure the accuracy of reading supplied by the supplier. A Fell's four-point probe is utilized for this operation; a probe spacing of 0.025" is used. Figure 7 illustrates the assembled equipment employed for resistivity measurements.

3. Radial Resistivity Gradient

This measurement is made employing the equipment seen in Figure 7 . This measurement is made on a silicon slice using a 0.025" Fell's four-point probe. Readings are made in the center and at 1/2 radius, and the gradient calculated from the data obtained. This is to insure a uniform distribution of dopant atoms in the slice.

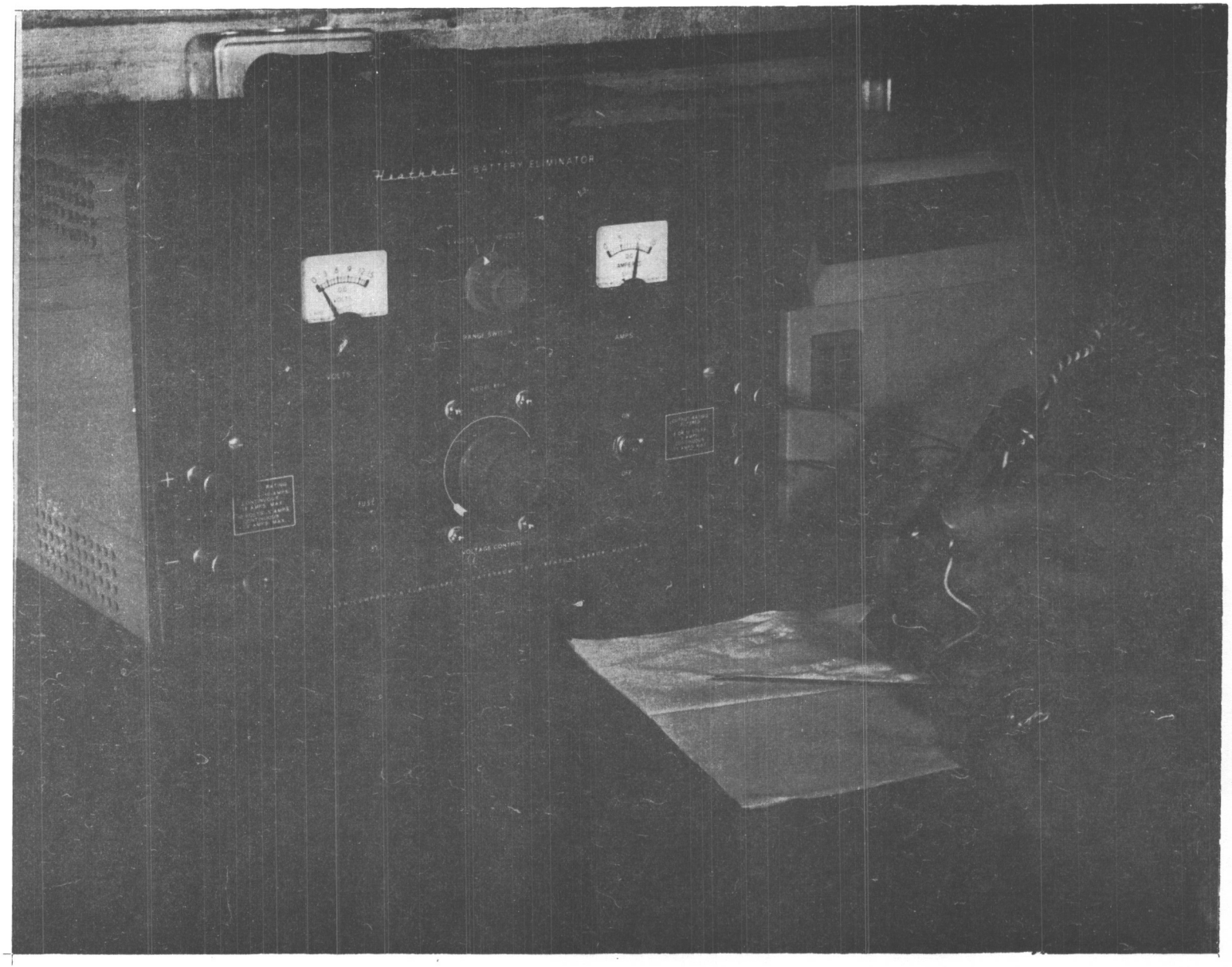


Figure 6: Thermoelectric Cold Probe

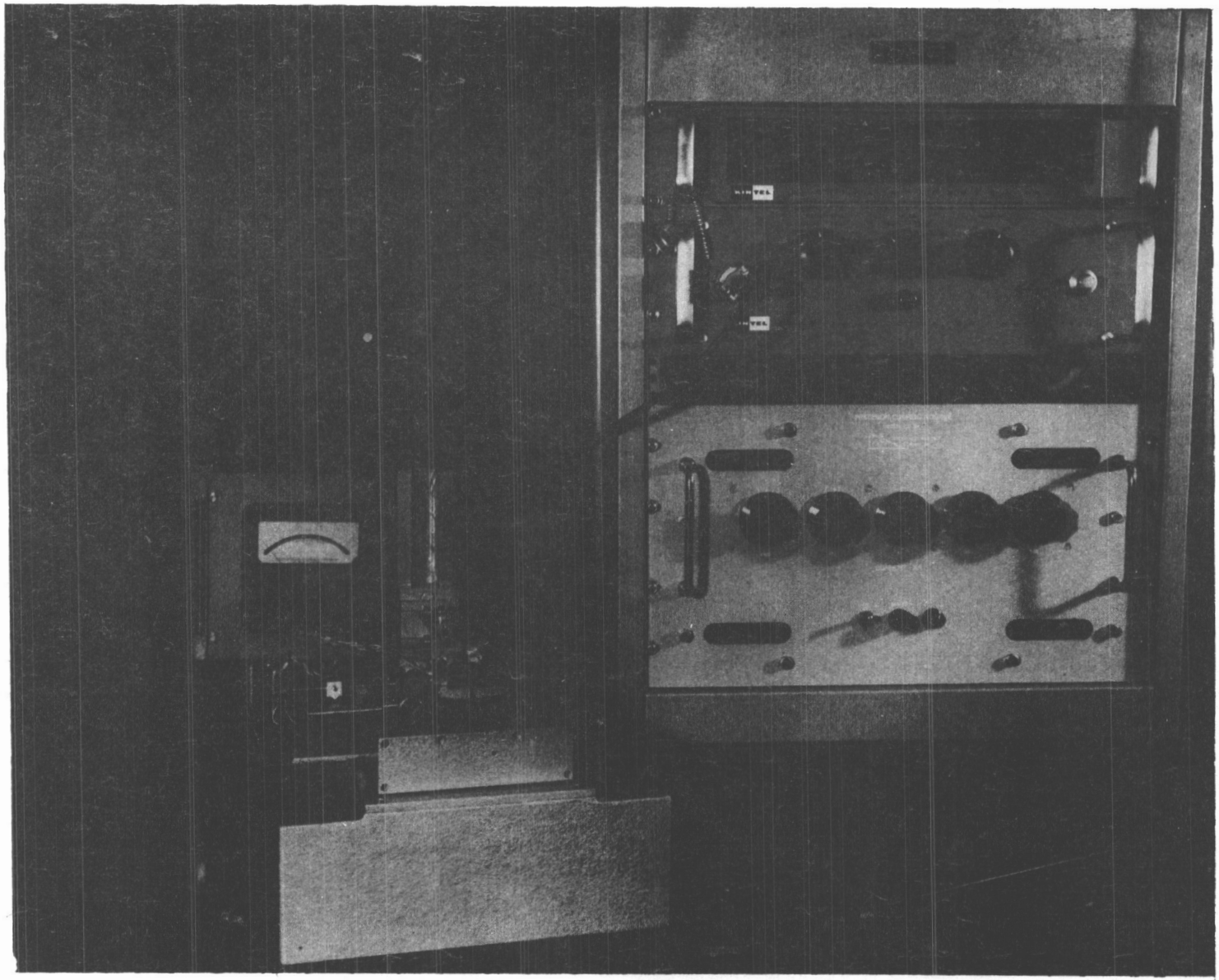


Figure 7: Resistivity Tester

4. Diameter

This material is centerless ground by the supplier to our specification. Buying the material to size eliminates the necessity of cavitroning, etching or sandblasting prior to epitaxial growth.

5. Dislocation Density

This parameter is checked on both the seed and the end of the crystal opposite the seed. These slices are etched in chromium trioxide to reveal the etch pits, and a count is then made to determine the number/cm^2. Figure 8 illustrates the microscope used to count the etch pits.

6. Orientation

A photograph of the orientation apparatus is shown in Figure 9. The primary objective is to insure that after sawing there will be a round slice of 0° on the (111).

7. Lifetime

The lifetime equipment is illustrated in Figure 10, which is a photoconductive decay instrument. The crystal is first degreased, washed with pure water and dried, the ends of the crystal are then gold plated to insure good electrical connection when it is placed in the above equipment. Known lifetime standards are checked daily.

8. Lineage

One slice is taken from the end of the crystal opposite the seed. This slice is then lapped using 12 micron grit size. Following lapping it is degreased and cleaned. The slice is then placed in a mixture of HF, H_2O, and Cr_2O_3 (1:1:1) for 5 minutes. The etch pit count is then made at 200X and the count reported in etch pits/cm^2.

9. Other Imperfections

The slice used in (8) is then relapped to remove the etch and is then re-etched but in a 10% solution of sodium hydroxide for a structural

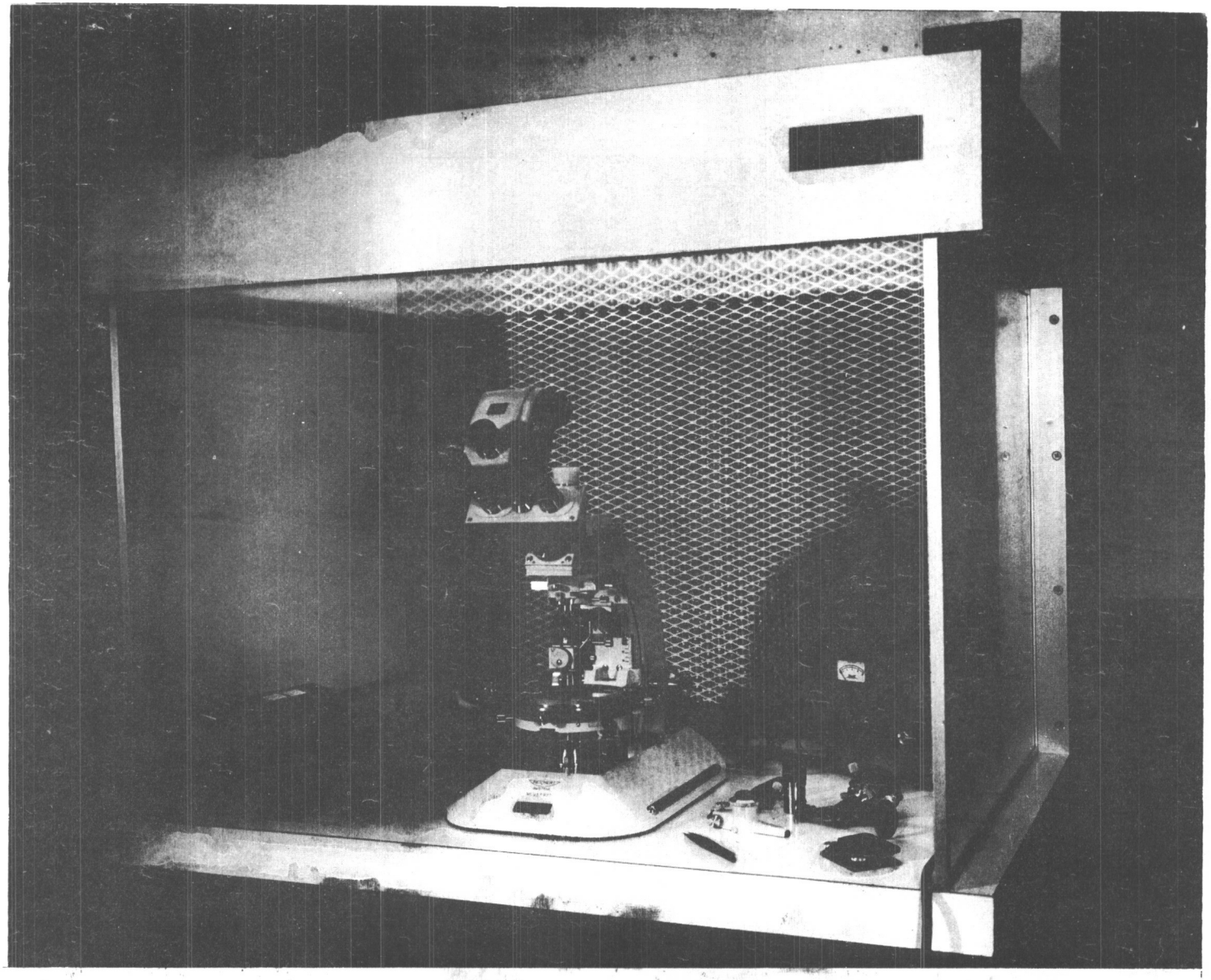


Figure 8: Normarski Interference-Contrast Microscope

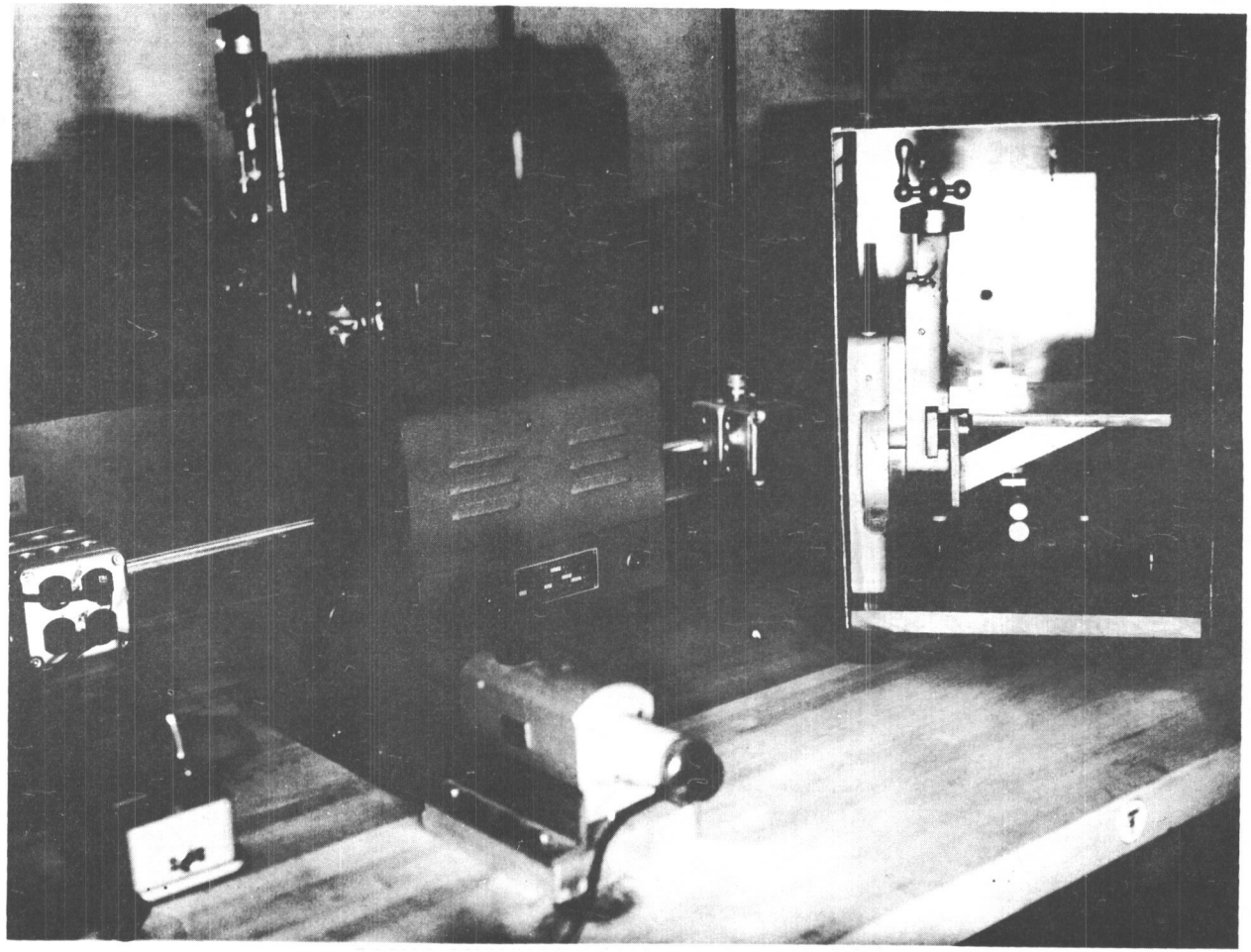


Figure 9: Orientation Apparatus

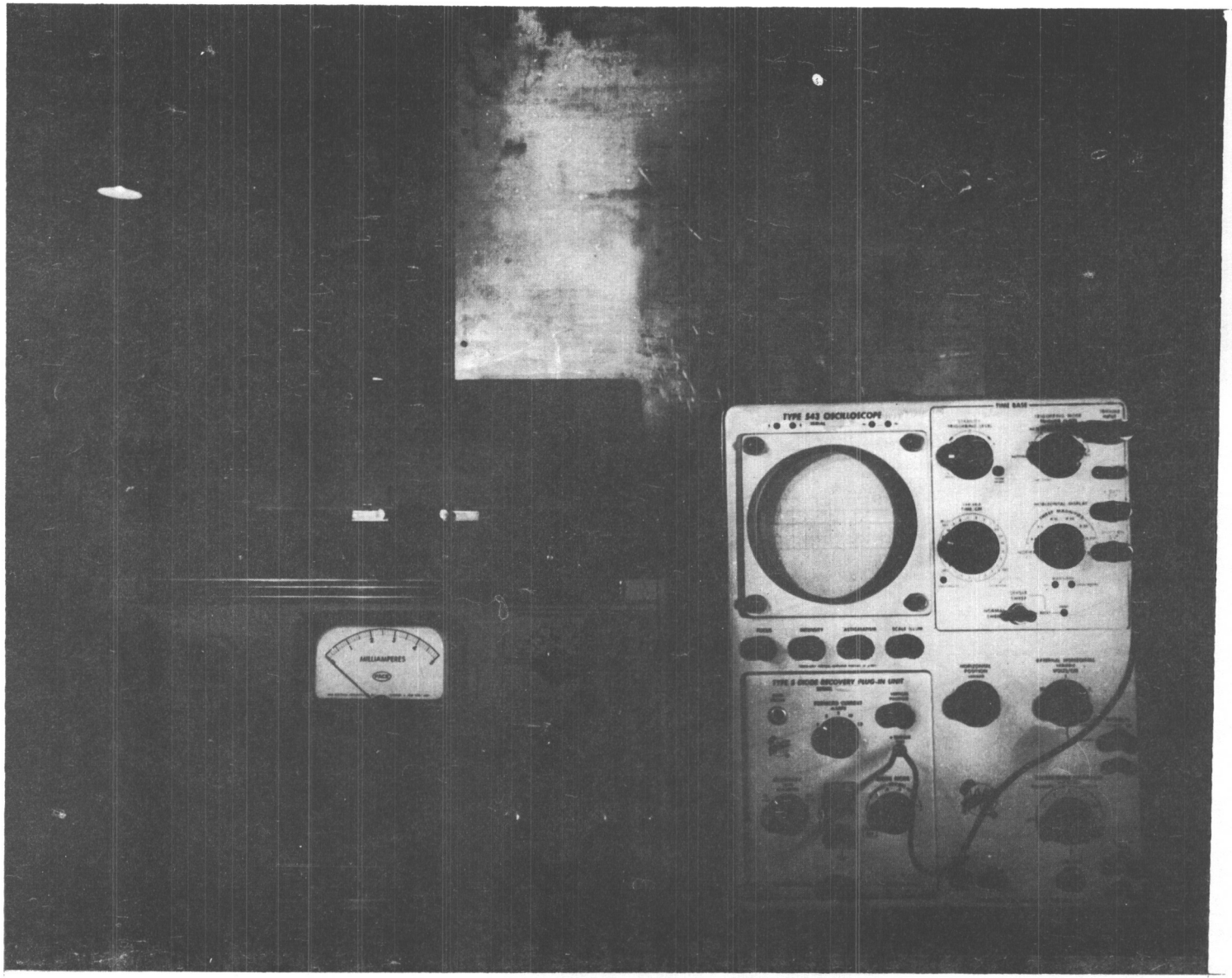


Figure 10: Lifetime Test Equipment

examination of the slice, where the primary imperfection might be twin-poly inclusions or slip.

E. MATERIAL PREPARATION

1. After the material has been evaluated and found to be in accordance with specification, it goes to the slicing area. Here the silicon crystal is sliced with a Hamco saw (See Figure 11), which according to our investigation, gives the best surface finish.

2. The slices are then forwarded to the lapping area where approximately 2 mils are removed from each side of the slice with a Hoffman planetary lapping machine (See Figure 12). The lapping slurry used is approximately 12 micron grit size, which leaves a mat surface.

3. The lapped slices are cleaned and chemically polished in a 15:5:3 mixture of nitric acid, acetic acid and hydrofluoric acid, respectively. A rotating table is used for the chemical polishing operation to minimize edge rounding and "orange peel."

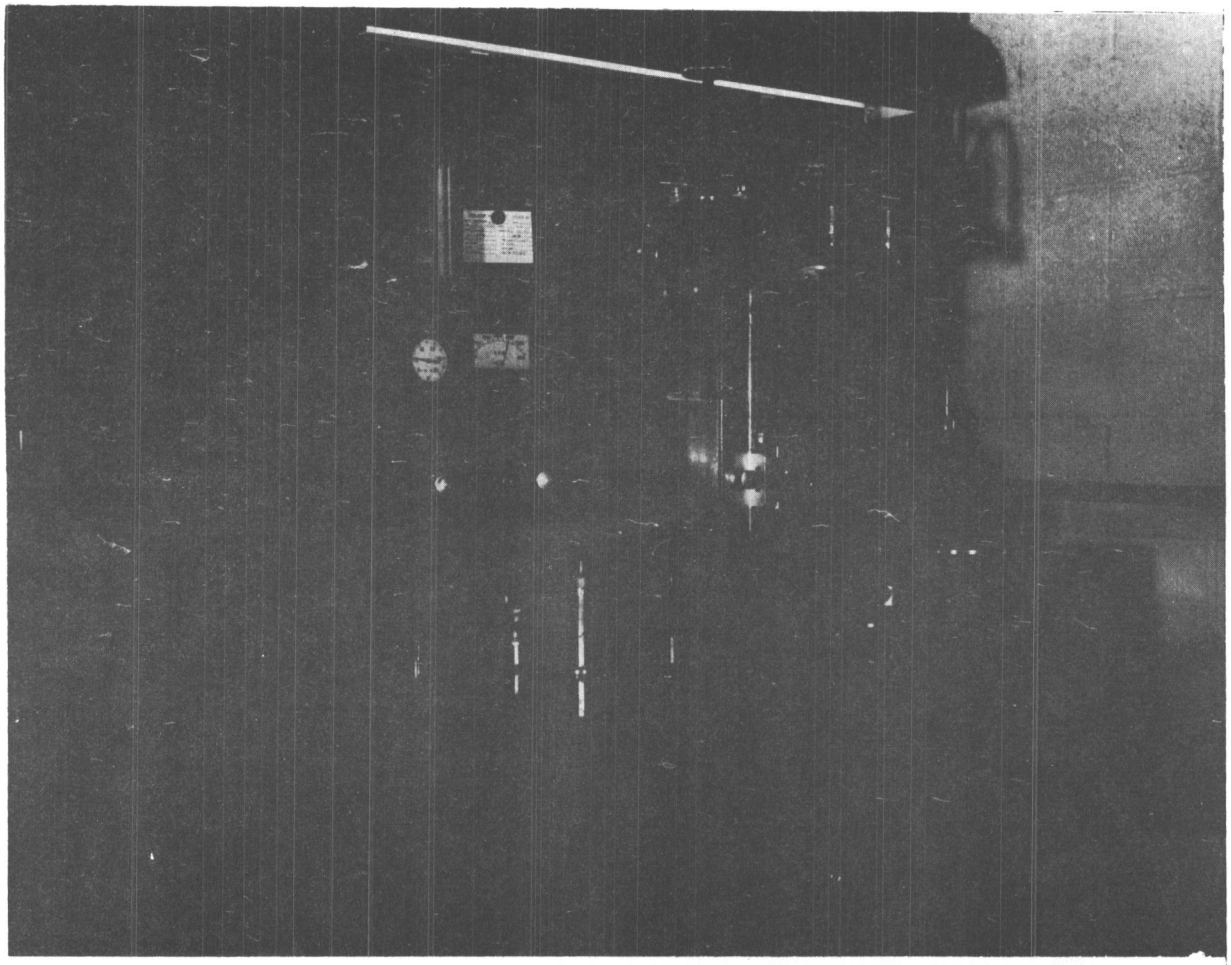
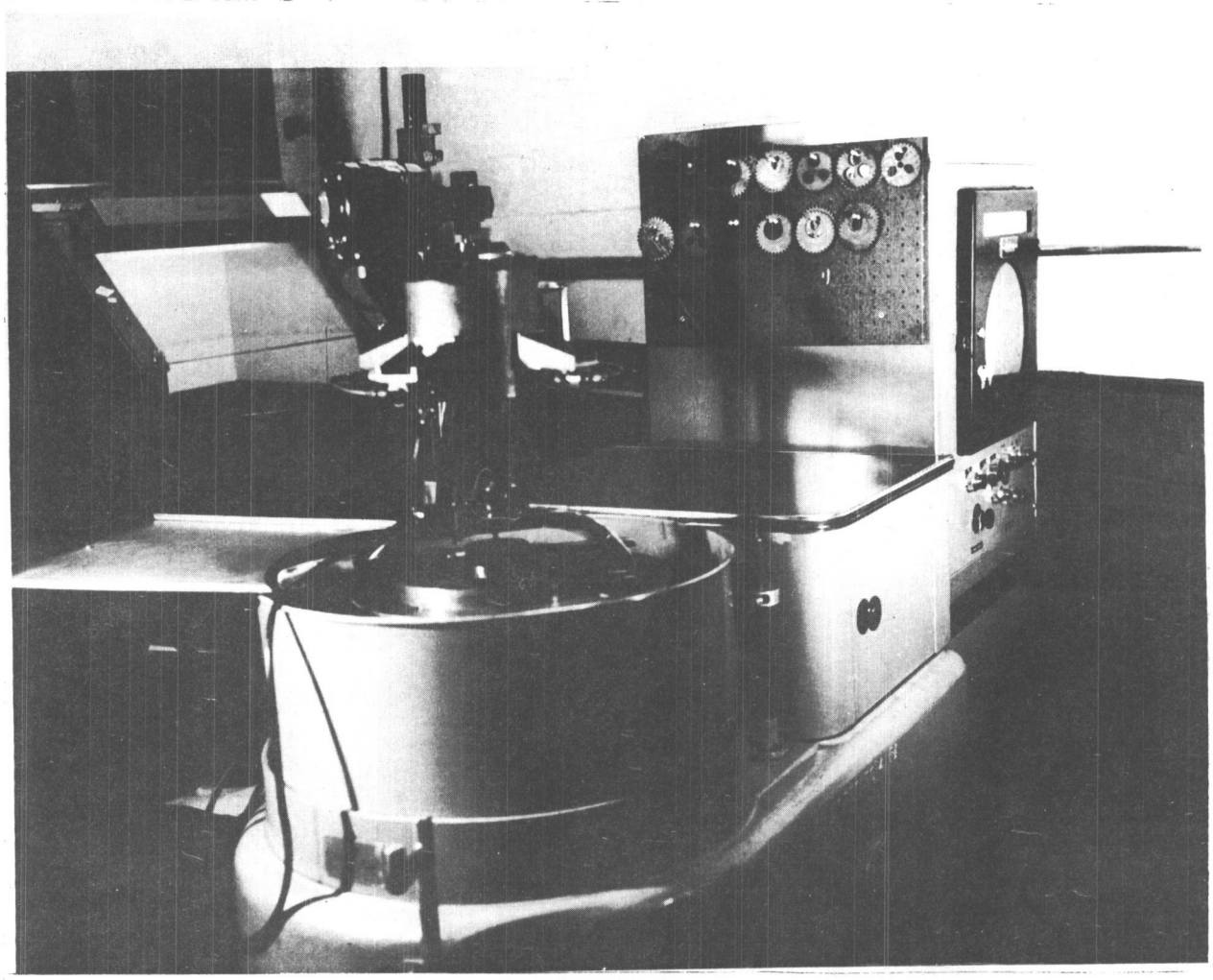


Figure 11: Hamco Cutting Saw



Planatary Lapping Machine

Figure 12:

IV. X-RAY TOPOGRAPHIC STUDIES

A. TECHNIQUES

In recent years, there has been a rapidly growing interest in the use of X-ray topography as a tool for the nondestructive assessment of imperfections in semiconductor and other crystals. The method, in principle, utilizes the phenomenon of enhanced diffraction from damaged regions of the crystal lattice. Although limited in resolution to the micron range, it provides a highly sensitive means of quality assessment. The single-crystal sample to be studied is irradiated by a high intensity, parallel beam of monochromatic X-rays at an angle which permits a strong Bragg reflection to be recorded on a photographic plate. This permits an image to be formed; the contrast effects in this image may be related directly to specific imperfections in the crystal sample. A photograph of the apparatus is shown in Figure 13 with a Lang camera mounted on the right-hand portion of the micro-focus X-ray generator.

B. RESULTS

The influence of two processing techniques was revealed by the X-ray studies. Figure 15 shows a wafer with only the epitaxial layer present. It can be seen to be essentially dislocation free. However, near the center is a linear arrangement of four small spots separated by 25 mils. This is the damage caused by testing with a four-point probe. The consequences of this damage are revealed in Figure 15 which shows this wafer after oxidation. The damaged region has acted as a source to generate innumerable dislocations. This central region deteriorates further during subsequent treatments.

The origin of other dislocations is shown in a comparison of Figures 16 and 17. The former is a wafer which has undergone processing while standing on edge and the latter is a wafer treated while lying flat. Although a high density of dislocations is present in both wafers in the central probed region, the second shows much fewer in other regions. It is concluded that

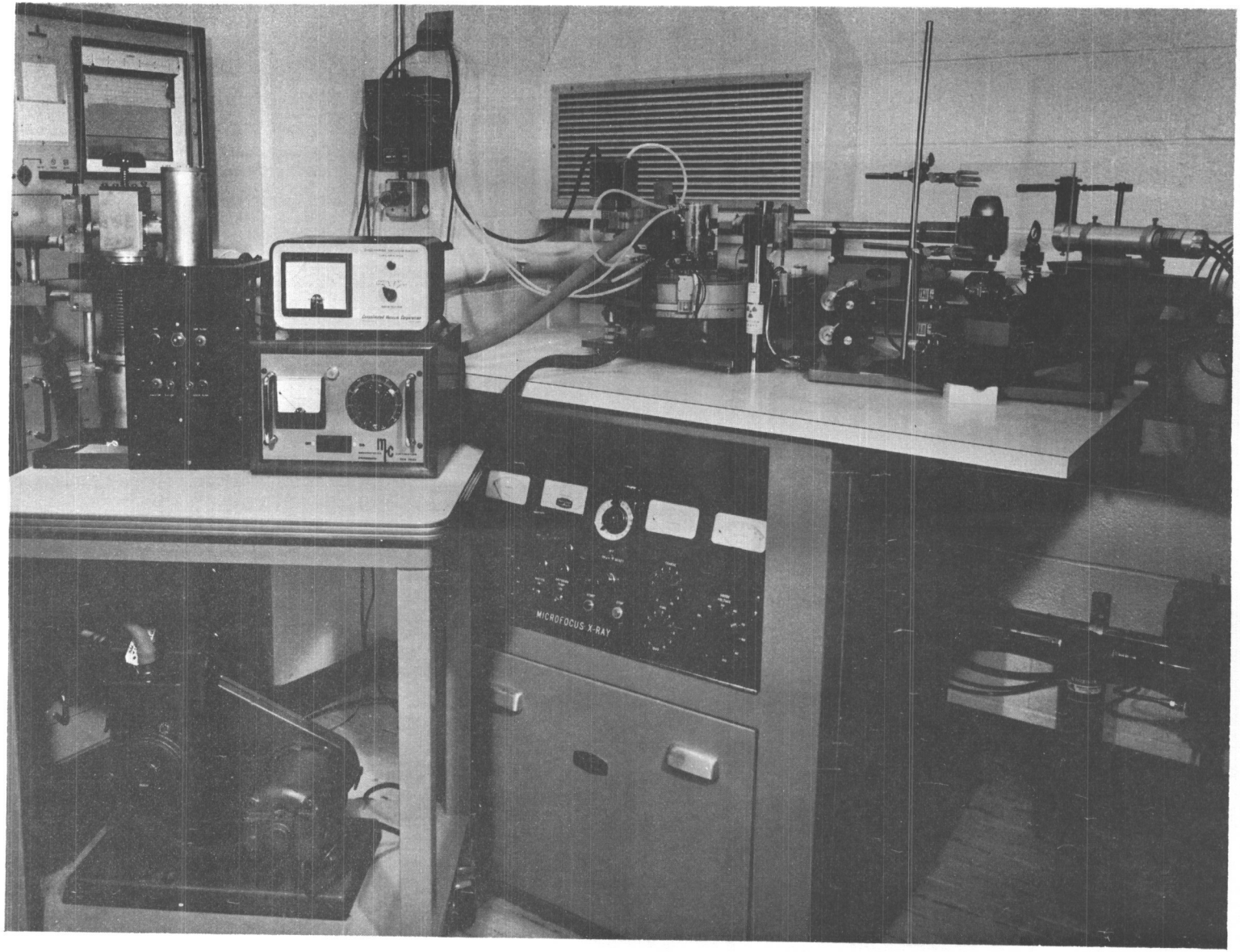


Figure 13: X-ray Topography System

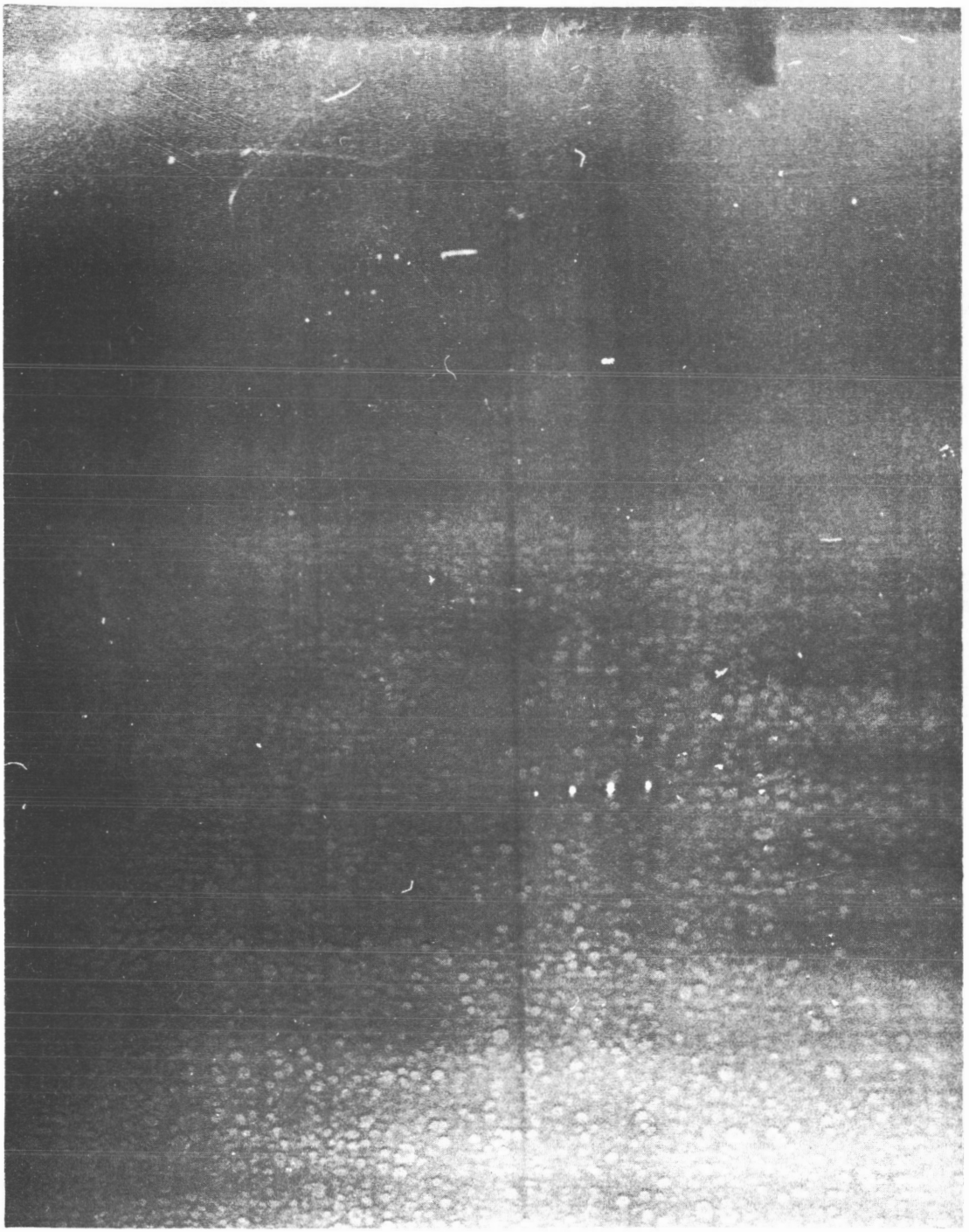


Figure 14: Topograph of Starting Wafer

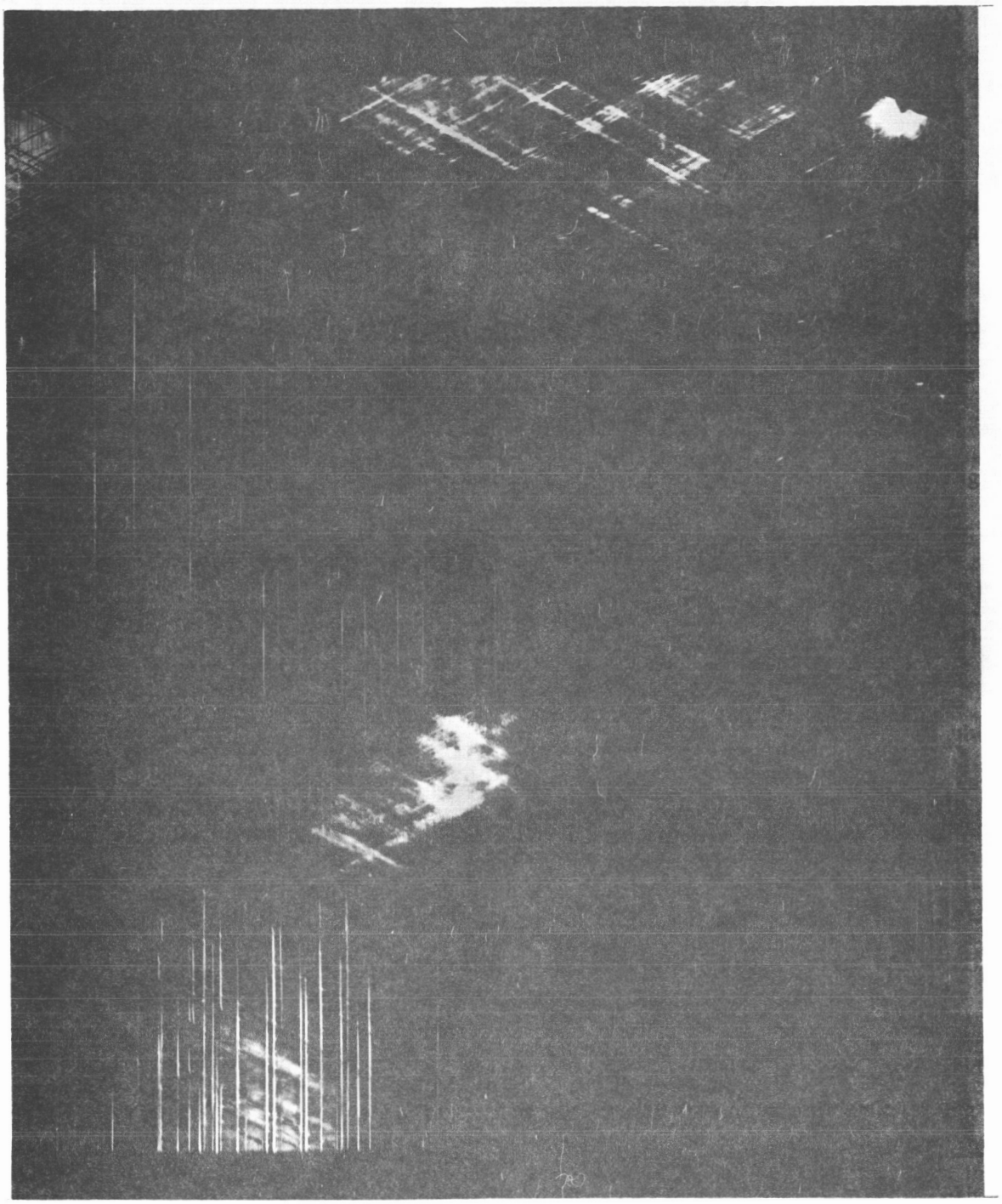


Figure 15: Topograph of Wafer After Oxidation

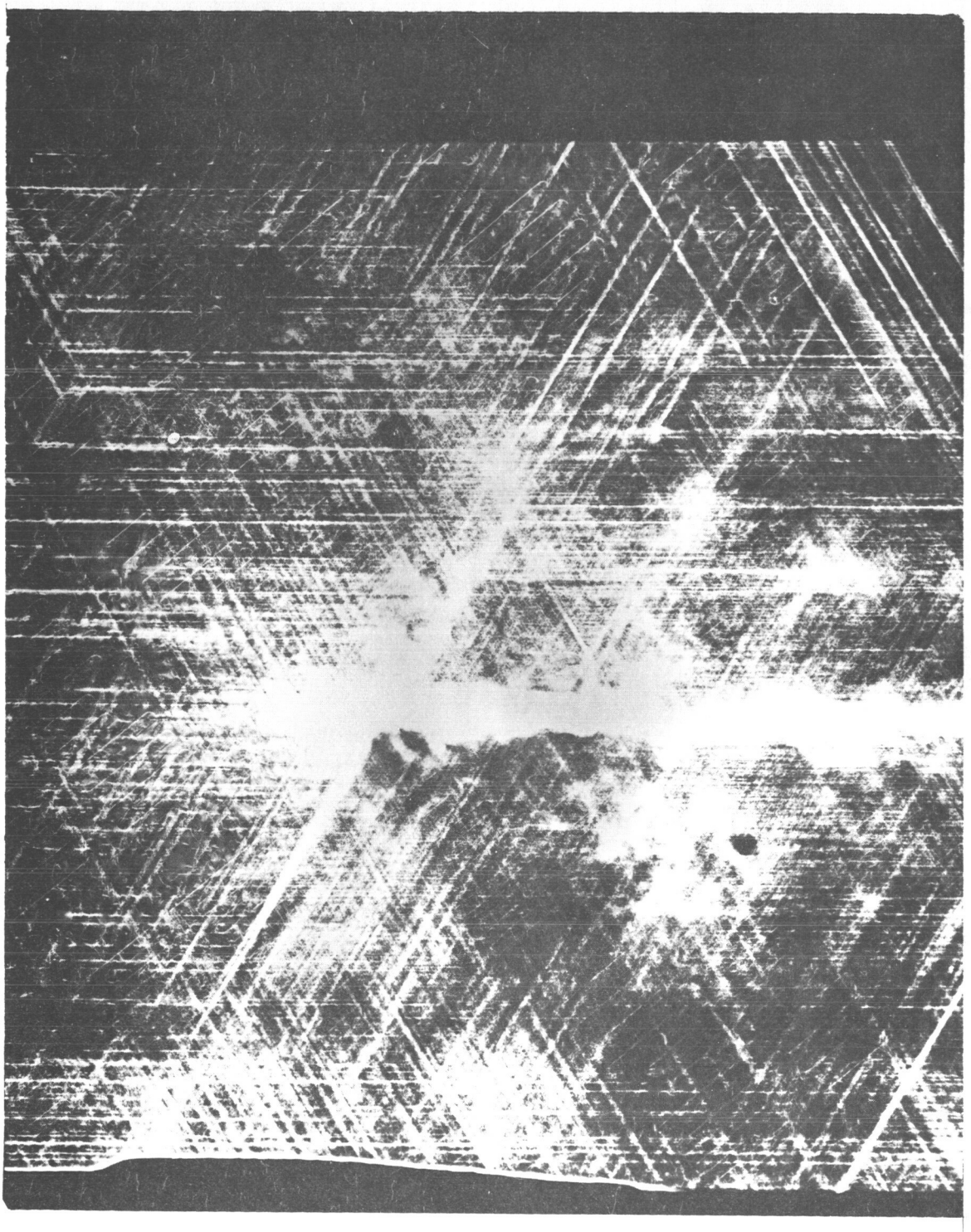


Figure 16: Topograph of Wafer Processed While Standing on Edge

Figure 17: Topograph of Wafer Processed While Lying Flat

many dislocations result from the strain exerted by standing a wafer on edge while undergoing thermal processing.

C. DISCUSSION

The ultimate objective of the X-ray studies is to correlate device degradation with defects either in the starting material or process induced. In the present study, the results have been dominated by two major types of process damage which may have little direct bearing on the nature of the correlation sought as they may be distributed through the bulk of the wafer. The first is the influence of probe damage. The second is apparently due to edge dislocations generated by plastic deformation, resulting from the sample position during processing. Both types can be minimized or eliminated and/or the X-ray technique modified. This would permit study of the more subtle effects associated with the various processing stages and subsequent correlation with device performance.

V. FABRICATION

A. PROCESSING

The initial phase of this study involved the fabrication and evaluation of 30-ampere epi base transistors. The transistor geometry utilized has 2.9 inches of emitter edge on a chip 250 mils square. Figure 18 is a flow chart showing the process sequence. Encapsulation and evaluation for both the 30- and 100-ampere versions will be discussed in later sections. Figure 19 is a flow chart for the 100-ampere transistor.

The first process step after epitaxial growth is oxidation. The purpose of this operation is to provide a SiO_2 layer thick enough to mask against subsequent diffusions. The first diffusion is a P^+ BBr_3 diffusion which serves to reduce r_{bb}'. For the 100-ampere transistor, this diffusion is done nonselectively. Thirty-ampere transistors were fabricated with selective and nonselective P^+ regions. The P^+ region serves to reduce $V_{CE(sat)}$ but has no effect upon the secondary breakdown performance of the device.

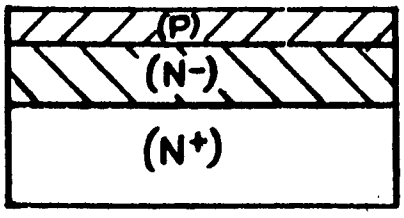
Prior to this diffusion operation, the wafers are subjected to a thorough pre-diffusion cleaning. This consists of soaking the wafers in hot sulfuric acid, hot nitric acid and hot filtered deionized water. The wafers are then blown dry with filtered nitrogen and loaded onto the diffusion boat. This sequence is repeated immediately prior to each diffusion operation. The actual diffusion and photomasking operations are performed in a dust-free atmosphere with controlled humidity and temperature.

The r_{bb}' reducing P^+ deposition is done at 1000°C for 5 minutes in an atmosphere of $BBr_{3(g)}$, $N_{2(g)}$ and $O_{2(g)}$. The resulting oxide is removed by etching in hydrofluoric acid. The wafers are cleaned and oxidized for 30 minutes at 1200°C in an atmosphere of $H_2O_{(g)}$ and $O_{2(g)}$. This produces

30 AMP 'EPI BASE' TRANSISTOR

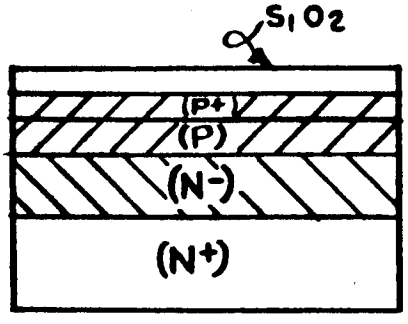
STARTING MATERIAL

.01Ω CM N TYPE, Sb DOPED
CHEMICALLY POLISHED
6-7 MILS THICK



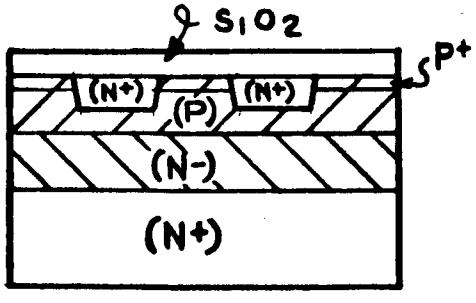
EPITAXIAL GROWTH

N- 20μ 11Ω CM.
P 5μ .5Ω CM.



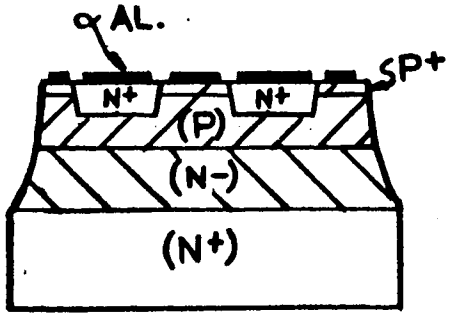
BORON DEPOSITION & OXIDATION

BBr_3 DEPOSITION - 1000°C 5 MIN.
OXIDATION - 1200°C 30 MIN.
P+ ρ = 150 Ω/□ X_J = 1μ
P+ REDUCES $r_{bb'}$



EMITTER MASKING & DIFFUSION

$POCl_3$ DEPOSITION - 1150°C 15 MIN.
OXIDATION - 1100°C 11 MIN.
N+ ρ = 2 Ω/□ X_J = 3.3μ W_B = 3.0μ



CONTACT MASKING & MOAT ETCHING

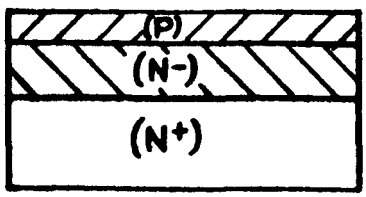
AL. EVAPORATION 40,000 A°

Figure 18: 30-Amp Flow Chart

100 AMP. EPI BASE TRANSISTOR

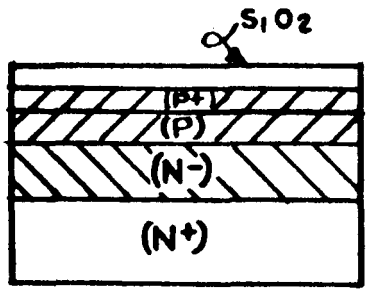
STARTING MATERIAL

.01 Ω CM N TYPE, Sb DOPED
CHEMICALLY POLISHED
6-7 MILS THICK



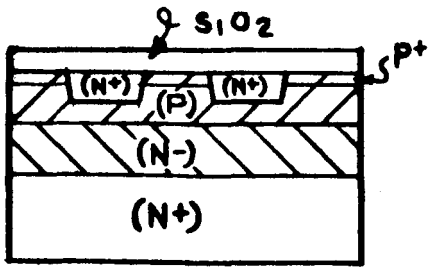
EPITAXIAL GROWTH

N- 20μ 11 Ω CM.
P 5μ .5 Ω CM.



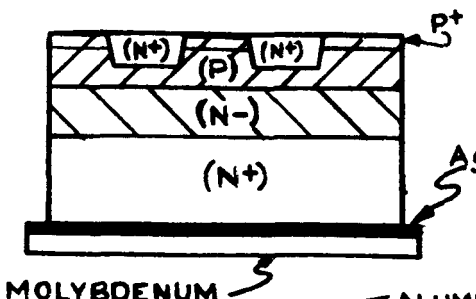
BORON DEPOSITION & OXIDATION

BBr_3 DEPOSITION - 1000°C 5 MIN.
OXIDATION - 1200°C 30 MIN.
P+ ρ = 150 Ω/□ X_j = 1μ
P+ REDUCES $r_{bb'}$



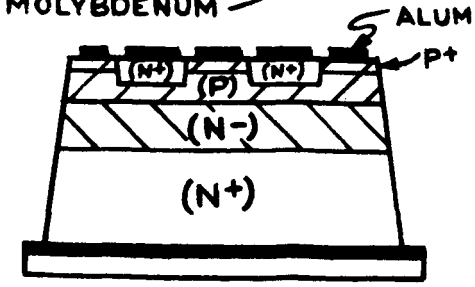
EMITTER MASKING & DIFFUSION

$POCl_3$ DEPOSITION - 1150°C 15 MIN.
OXIDATION - 1100°C 11 MIN.
N+ ρ = 2 Ω/□ X_j = 3.3μ W_B = 3.0μ



MOUNT SILICON ON MOLYBDENUM

TEMPERATURE 880°C



EVAP. AL., ANGLE BLAST EDGE SPIN ETCH, & COAT

Figure 19: 100-Amp Flow Chart

an SiO_2 layer 7000Å thick, which is sufficient to mask against the subsequent emitter diffusion. The P^+ region has a sheet resistivity of 125 to 150 ohm/□ . If this region were made more concentrated, r_{bb}' would be reduced still further, but so would V_{EBO}. This concentration yields $V_{EBO} \cong 7.5V$.

Initial runs were made with the wafers standing up in the diffusion boat. This is desirable from a capacity standpoint. However, X-ray topography studies indicated that dislocations were being generated so that later runs were made with the wafer laying flat on the diffusion boat. The relationship between device performance and these dislocations has not been established. It is possible that these dislocations are deep within the wafer and do not effect device properties. This subject is discussed in greater detail in another section.

After the initial oxidation, the 30-ampere transistor wafers are ready for emitter masking. The 100-ampere transistor wafers must now be sandblasted to size. This initial wafer is 1.3 inches in diameter to insure epitaxial layer uniformity. It is well known that variations within epitaxial layers are pronounced near the edge of a wafer due to variations in reactant gas flows at the wafer-gas stream interface. This 1.3-inch wafer is sandblasted on a rotating fixture to .94 inch. This is done prior to emitter photomasking to insure maintenance of the radial symmetry of this device geometry.

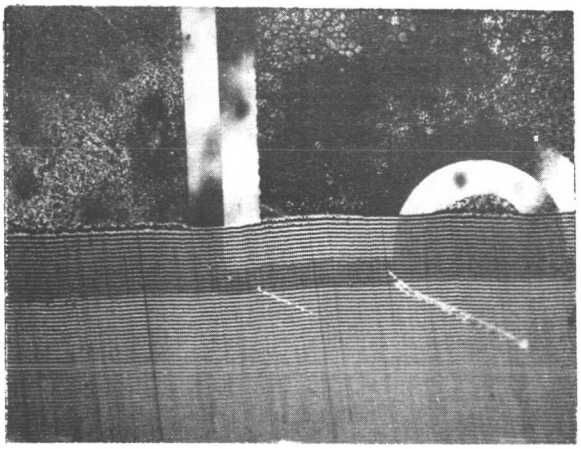
The compression bond encapsulation techniques employed necessitate precise location of contact regions, which are fixed by the emitter mask. The sandblasting operation is done after oxidation to minimize damage to the Si surface. For further protection, the wafer surface is coated with a dental wax during sandblasting. After sandblasting the wafers are cleaned for photomasking.

The purpose of the emitter photomasking step is to define the emitter geometry on the wafer. This is done by selectively exposing a photosensitive film with ultraviolet light and subsequently etching the uncoated SiO_2 with HF. The SiO_2 that is not removed will mask against the subsequent phosphorus emitter diffusion. Commercially available KMER is used for this purpose. The KMER is forced through a 7μ membrane filter onto the wafer. A uniform film is obtained by spinning the coated wafer for 1 minute at 4000rpm. The coated wafer is baked for 10 minutes at 95°C in an air oven. The wafer is then aligned and exposed using a conventional alignment fixture. The unpolymerized resist is then removed by spraying with a developer and then with isopropyl alcohol. The unprotected oxide is then removed by etching in a buffered hydrofluoric acid solution. After etching is complete, the photoresist is removed with trichloroethylene or hot sulfuric acid.

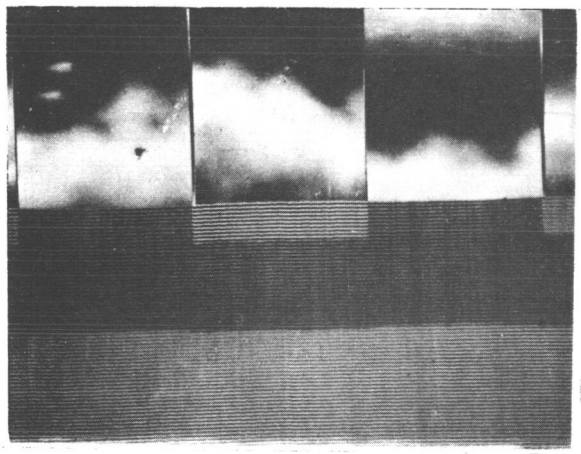
The emitter diffusion is done at 1150°C in an atmosphere of $POCl_{3(g)}$, $O_{2(g)}$ and $N_{2(g)}$. The time is determined by the epitaxial P-layer thickness and the desired base width. After this diffusion, the wafers are oxidized at 1100°C. This serves to dilute the phosphorus glass formed during the $POCl_3$ diffusion. It is difficult to obtain photoresist adhesion to this phosphorus glass. This low temperature oxidation doesn't decrease the base width since this is determined by the 1150°C $POCl_3$ diffusion. It does, however, serve to activate any electrically inactive phosphorus in the heavily doped emitter region. This provides greater device stability.

The emitter diffusion is evaluated by conventional sectioning and resistivity measuring techniques. Figure 20 shows typical cross sections of three different base widths.

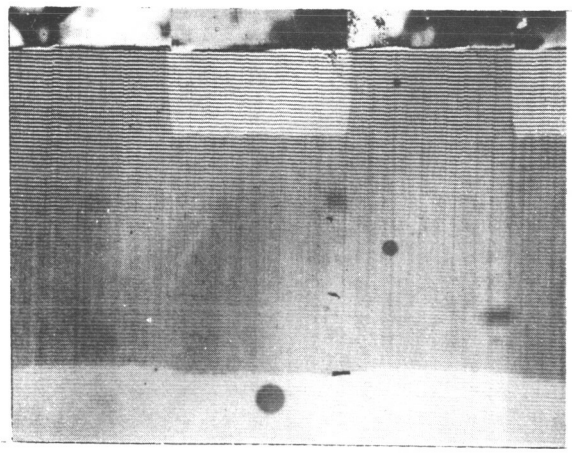
Contact photomasking serves to remove the oxide from the emitter and base contact areas. The 100-ampere transistors are then mounted on a molybdenum disc using a Ag-Pb-Sb solder. This is done in a vacuum of less than 10^{-6} Torr at 860°C.



3.3μ W_B



7.5μ W_B



18.0μ W_B

Figure 20: Typical Cross Sections

Molybdenum mounting is a critical process step in that device performance is strongly dependent upon a uniform wetting of the collector area. It has been reported that solder voids can cause hot spots due to current crowding during device operation. These hot spots could cause the unit to fail under test. It is difficult to determine whether secondary breakdown or hot spots caused device failure during conventional evaluation. X-ray evaluation techniques have indicated the Westinghouse moly mounting technique produces void-free hard solder joints. Device failure therefore is most often caused by secondary breakdown rather than by the hot spot mechanism resulting from faulty mounting.

The moly mounted 100-ampere devices and the 30-ampere wafers both utilize an evaporated Al film for ohmic contact to the emitter and base areas. The devices are heated to 500°C in a vacuum of less than 10^{-6} Torr within the evaporator to insure the clean surface necessary for adhesion of the Al to the Si surface. The devices are allowed to cool to less than 100°C before 40,000Å of Al is evaporated using conventional techniques.

During inverse contact etching, it is necessary to protect the moly disc from attack by the Al etch. The inverse contact photoresist step serves to remove the nonselectively evaporated Al from other than the previously defined contact areas. When this is done the wafers are alloyed at 580°C in a dry nitrogen atmosphere. This alloying step forms a thin region of an Al-Si eutectic in the contact areas and insures an ohmic contact.

Since the epi base technique produces a nonselective base region, a mesa etch is necessary to develop the C-B and C-E voltages. This is done using conventional photoresist techniques. Again it is necessary to protect the moly disc of the 100-ampere transistor. Immediately after mesa etching a passivating silicone-alizarin coating is applied to the exposed C-B junction of the 100-ampere transistor. After this step, the 100-ampere devices are

ready for testing and encapsulation. After the mesa is etched on the 30-ampere wafer, the slice is ready for slice test, scribing and dice test. Electrically acceptable transistor chips are mounted to gold plated TO-63 bases and leads are ultrasonically attached before the protective coating is applied to the exposed junction. The assembly is now ready for encapsulation.

B. CONTACT DESIGN

It has long been recognized that excessive localized stresses on a compression bonded device will cause downgrading or even complete failure of the device. Due to the narrow emitter contacting surface, the subject device was especially subject to excessive localized stresses.

In order to spread the compression force required for encapsulation over the whole surface of the device, a search was made for a material with mechanical, electrical and thermal characteristics suitable for intimate contact with the surface of the device. One material that was readily available and uniquely suited to the requirements was Teflon*, type TFE (polytetrafluorethylene).

The literature[1] shows that parts made of TFE deform in time at a decreasing rate. This property can best be explained by the concept of "Apparent Modules of Elasticity." This concept takes into account the initial deformation for an applied stress plus the amount of deformation that occurs with time. At a given compressive force and temperature the initial deformation of TFE occurs within the first few hours. The deformation then levels off to a point where it is negligible.

The electrical properties of TFE in the required thickness far exceed the electrical characteristics of the devices. Sleeving of Teflon is

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* Registered trademark of E. I. DuPont de Nemours and Company.

(1) Teflon fluorocarbon resins, Mechanical Design Data, Plastics Department, E. I. DuPont de Nemours and Company, Wilmington, Delaware; Fluorocarbon Plastics - Materials and Process Manual, Materials in Design Engineering, February 1964.

already being used as lead wire insulation inside many of the Westinghouse transistors and controlled rectifiers.

The above-mentioned literature shows that TFE is useful from -267°C to +260°C. This far exceeds the rating of the subject device. Since TFE is enert to almost all chemical reactants it is an ideal substance to mate to the entire surface of the device.

The characteristics of Teflon were put to good use in the design of the base and emitter contacting elements of this device.

The emitter contacting element is shown in detail in Figure 21 . It consists of a washer of Teflon with a silver foil wrapped around the outside diameter so that contact is made on the bottom with the emitter contact area of the basic transistor and on the top to the larger emitter lead. The foil was formed around the outside diameter of the Teflon washer in the form of an arch to allow for the stress-strain characteristics of the Teflon.

When force was applied to the Teflon, it deformed plastically and elastically in all directions to conform to the configuration of the surfaces which opposed it. This deformation took place at a decreasing rate so that in a short period of time a semi-rigid state was reached that transmitted the force of the Belleville washers evenly over the whole surface of the transistor element.

Evidence of the deformation has been observed on contacts removed from devices by the impression of the surface of the basic transistor on the mating surface of the Teflon washer.

The base contact (Figure 22) was designed to make use of the inward expansion of the emitter washer. By machining a reverse chamfer on the base contact, the emitter Teflon was guided over this chamfer so that a

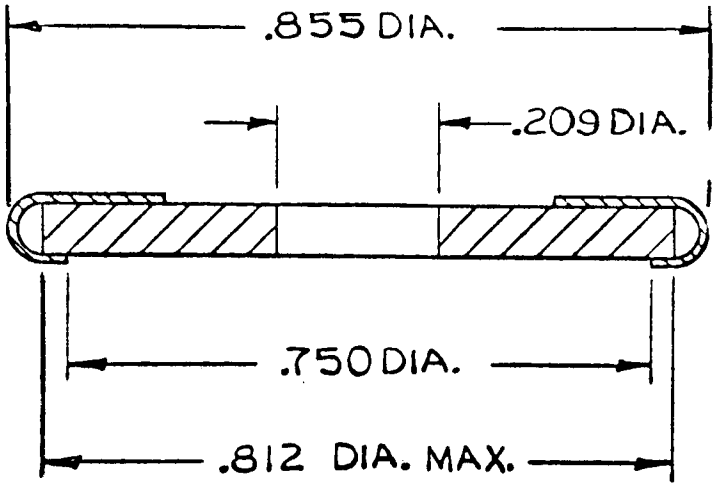
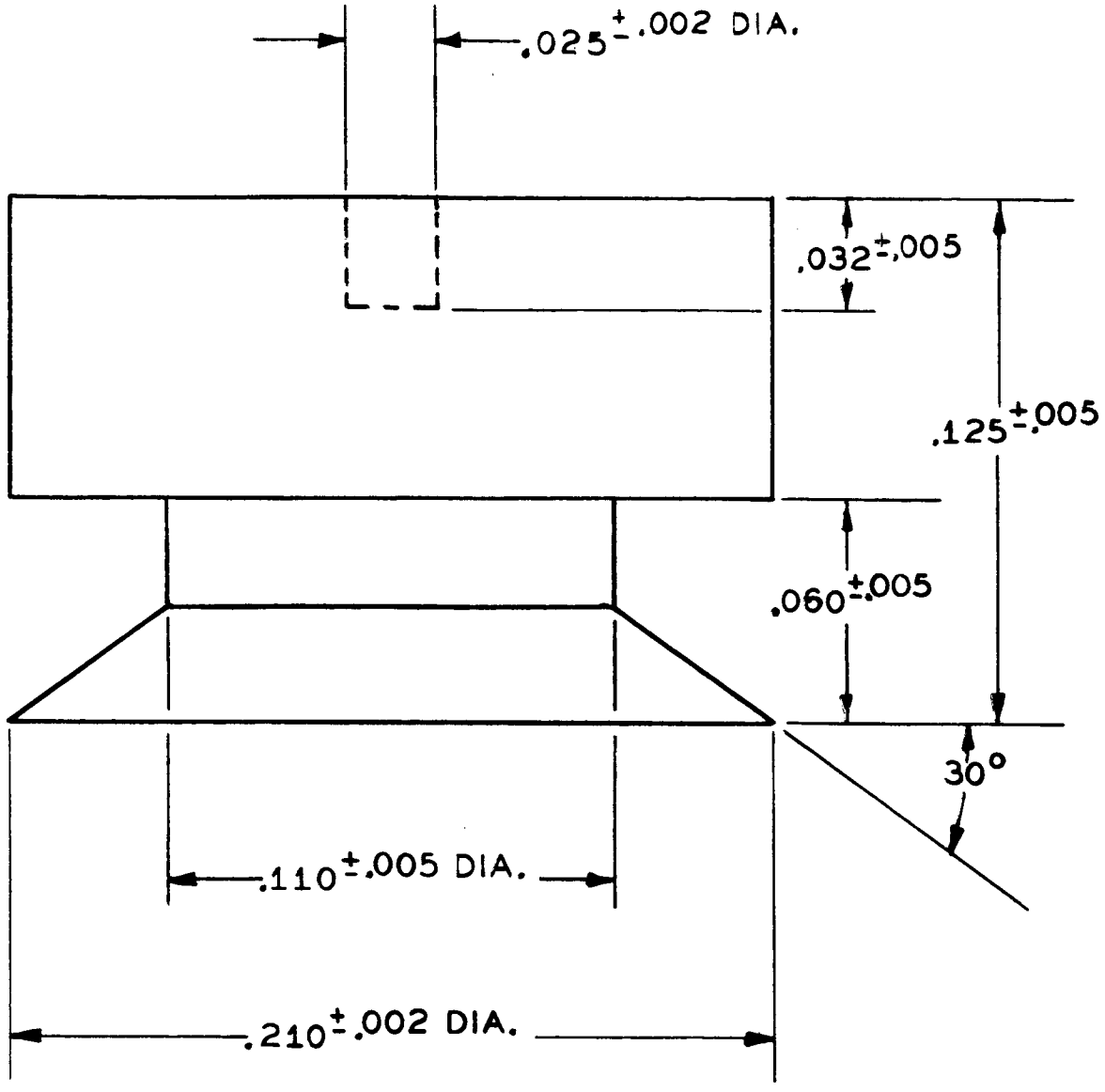


Figure 21: Details of Emitter Contact



NOTE

NO BURR OR PROJECTION ON BOTTOM SURFACE

MATERIAL — SILVER

FIGURE 22 (BASE CONTACT)

part of the force applied to the emitter by the Belleville washers was used to apply force to the base contact. A Teflon sleeve was inserted into the inside diameter of the emitter lead to insulate the base contact.

It was very important in designing the collector contact, to keep in mind that it was through this contact that the heat generated within the basic fusion flowed to be dissipated in the base and heat sink. This required that the molybdenum mounting disc of the basic fusion and the base be in intimate contact. To enhance the intimate contact between the basic fusion and the base, a lead soft silver disc was placed between them. The purpose of this disc was to fill as many voids (due to lack of flatness and surface finish) as possible in both the molybdenum mounting disc and pedestal surface.

Upon examining the foil after disassembly, the imprint of the molybdenum and the base surface irregularities were clearly visible; indicating that the silver foil was performing as intended.

C. DEVICE COMPONENTS

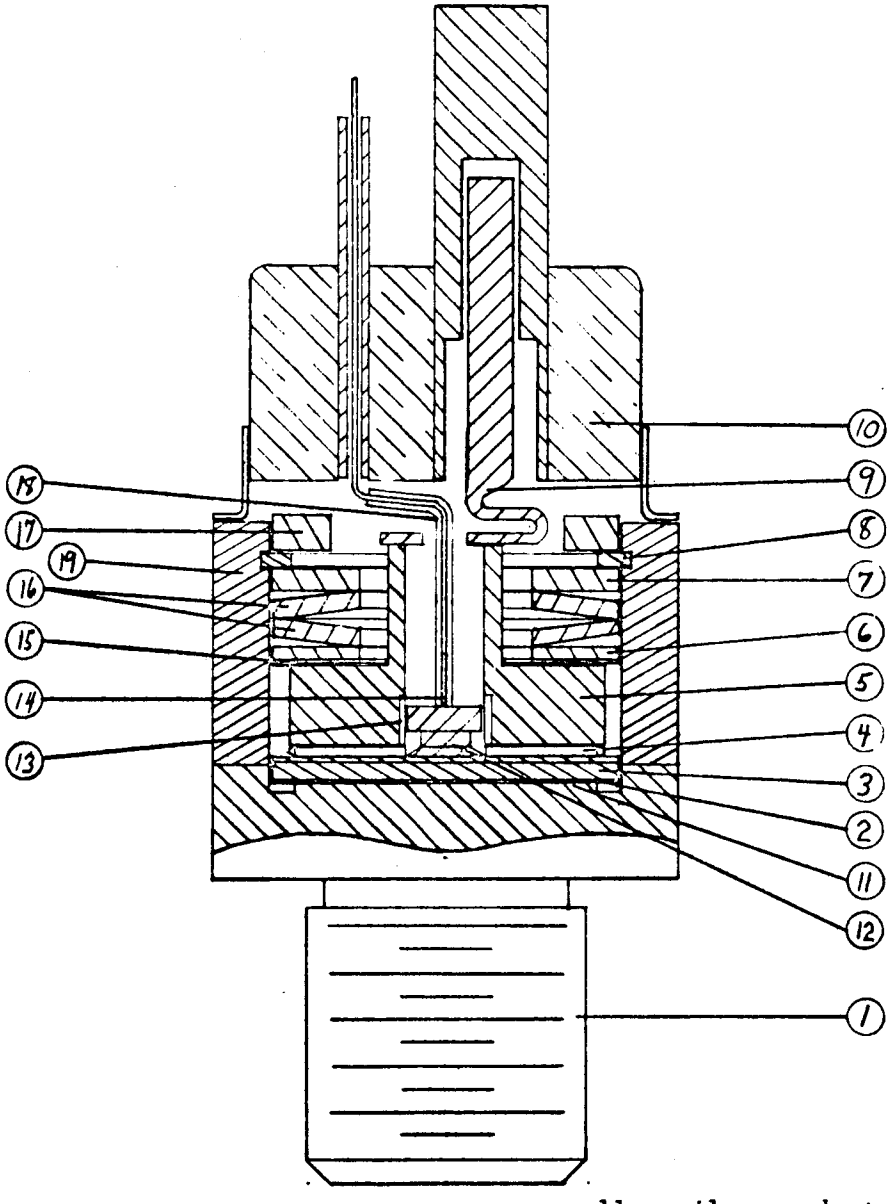
The components of the subject device are shown in Figure 23. Following is a brief description of each.

1. Base

Machined from P.D. 135, it provides a threaded stud to attach to a heat sink, a good thermal path from basic fusion to heat sink, and a pedestal on which the basic transistor is mounted.

2. Integral Case

Externally it provides the hex to hold or tighten the device to a heat sink and the weld projection to which the ceramic-metal seal is welded. Internally it locates the compression components and contains the groove for the retaining ring that maintains force on the device.



1. base
2. silver foil
3. basic transistor
4. emitter contact
5. emitter lead
6. flat washer
7. flat washer
8. retaining ring
9. silver emitter lead
10. ceramic-metal seal
11. silver pedestal
12. base contact
13. Teflon insulation
14. base lead wire
15. mica insulation
16. Belleville springs
17. molecular sieve
18. base lead insulation
19. integral case

Figure 23: Components of 100-Amp Encapsulation

3. Silver Braze

Means for attaching the silver disc to the pedestal.

4. Silver Foil

Provides the mounting surface for the collector side of the basic fusion. It is brazed to the pedestal of the base and then machined flat. A second silver foil is used as a cushioning disc to allow intimate contact between the silver foil on the pedestal and molybdenum of the basic device, thereby lowering the contact resistance.

5. Emitter Contact Assembly

Consists of a Teflon washer with a thin silver foil wrapped around the O.D. to make contact to the emitter lead on top and the narrow contact surface of the device.

6. Emitter Lead

This component transfers force to the top of the emitter contact assembly and makes contact with it. The center portion encloses and locates the base contact components.

7. Base Contact

A silver button with a reverse chamfer which allows the Teflon of the emitter contact assembly to flow over and up the chamfer, thereby holding it in place and providing the force to assure proper contact.

8. Base Lead Wire

Provides the connection between the base contact and ceramic-to-metal seal.

9. Base Contact Insulation

Insulates the base contact from the emitter lead and helps locate the base contact.

10. Base Lead Wire Insulation

Insulates the base lead wire from the emitter and collector portions of the device.

11. Mica Insulation

Isolates the emitter and collector regions of the device.

12. Flat Washer

Provides a flat bearing surface for the Belleville washers; and by exchanging washers of various thicknesses, the proper force may be maintained on the device.

13. Belleville Springs

Used in this device as two in series to provide the required force on the device.

14. Flat Washer

A .060" thick steel washer used to maintain the force on the device after it is removed from the press.

15. Retaining Ring

When force is applied to the device in the press, the retaining ring is snapped in place in a groove in the inner wall of the integral case. This ring prevents the springs from relaxing when force is removed.

16. Molecular Sieve

A moisture getter that is placed in the device to prevent downgrading due to moisture contamination.

17. Ceramic-To-Metal Seal

Welded to the integral case, it provides a hermetic seal and the means of attaching external leads to the emitter and base.

D. PRE-ENCAPSULATION PROCEDURE

All components except the mica insulators are thoroughly degreased in trichloroethylene. The mica is baked and stored in vacuum at 150°C for 12 hours prior to assembly.

1. A silver disc is placed inside the integral case and seated on the pedestal of the base.

2. A basic transistor element is seated on the silver foil.

3. The Teflon insulating sleeve is placed over the base contact.

4. A Teflon insulating tube is placed over the base lead wire.

5. The base lead is inserted through the inside diameter of the emitter Teflon contact, centered and the insulating sleeve (Step 3) is seated against it.

6. The emitter lead is placed over the gate lead wire and the base contact and Teflon insulation seated in the counterbore of the inside diameter.

7. Mica, a .035" thick flat washer, two Belleville springs in series with bottom washer concave, and a .060" thick flat washer are seated in turn on the top of the fusion.

8. The base with the loose assembly is placed in a Carver Laboratory Press and a force of 700-900 lbs. is applied.

9. The retaining ring is snapped in place and the pre-encapsulated device removed from the press.

10. After the pre-encapsulated assembly passes a series of electrical tests, it is passed on to final encapsulation.

E. FINAL ENCAPSULATION PROCEDURE

For the final encapsulation procedure, the parts involved are prepared as follows. The ceramic-metal seal is leak tested, degreased and baked in vacuum at 175°C for 4 hours. The molecular sieve is baked at least 16 hours in vacuum at 300°C. They are then stored in vacuum at 150°C. The pre-encapsulated assembly is baked in air at 175°C for 4 hours prior to the final encapsulation.

All components in this section are shown in Figure 24.

Procedure

1. The molecular sieve is placed over the leads and seated inside the integral case on the snap ring.

2. The base lead wire is guided through the base lead connector as the ceramic-metal seal is placed over the emitter lead and seated on the weld ring.

3. The base lead wire is pinch welded inside the connector.

4. The ceramic-metal seal is resistance welded to insure hermeticity of the assembly.

5. The emitter lead connector is then crimped in place.

6. The device is leak tested and plated with nickel.

The final encapsulation is then complete and the devices are ready for final electrical testing.

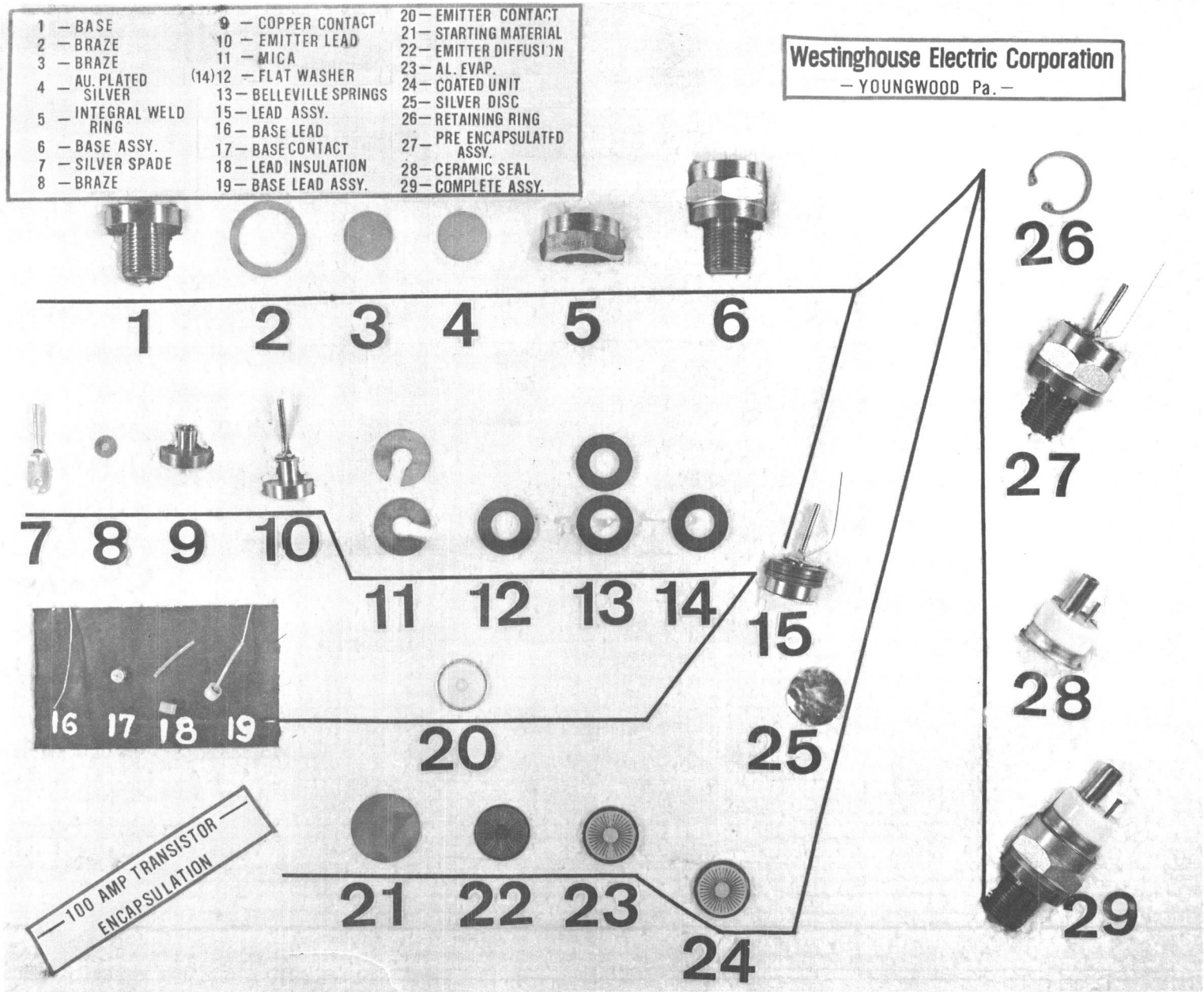


Figure 24: 100-Amp Transistor Encapsulation

VI. TESTING AND ELECTRICAL RESULTS

A. ELECTRICAL TESTING

The electrical evaluation of the transistors fabricated for this study necessitated the development of special test circuits because of the relatively high frequency response and fast switching characteristics. Electrical characterization must be done under precisely defined test conditions to obtain valid results without destroying the transistor. For example, $V_{CEO(sus)}$ and $V_{CER(sus)}$ must be measured on the test circuit shown in Figure 25 and not on a curve tracer. This test set will sweep the transistor under test through an inductive load line to obtain the sustaining characteristic of the collector-emitter junctions. In operation, a modest current is passed through the transistor with an inductor in series with the collector. The transistor is then turned off very rapidly with reverse biasing and the inductor is discharged through the collector-emitter circuit. The discharge of this inductor will sweep the collector to a high voltage at approximately constant current in the collector until breakdown of the collector-emitter junction occurs in the sustaining mode. The sustaining characteristics are determined by observing this load line on an oscilloscope and reading the maximum voltage at the specified current. This equipment is also capable of performing V_{CER} sustaining tests.

With the circuit shown, the 20mH inductor limits the energy to the transistor by the equation $E = L\ di/dt$. The amount of inductance selected depends on the f_t of the transistor. Attempts to measure $V_{CEO(sus)}$ on a curve tracer will result in device failure with no information about the conditions which caused the failure.

To obtain quantitative information about device failure, other test procedures are used.

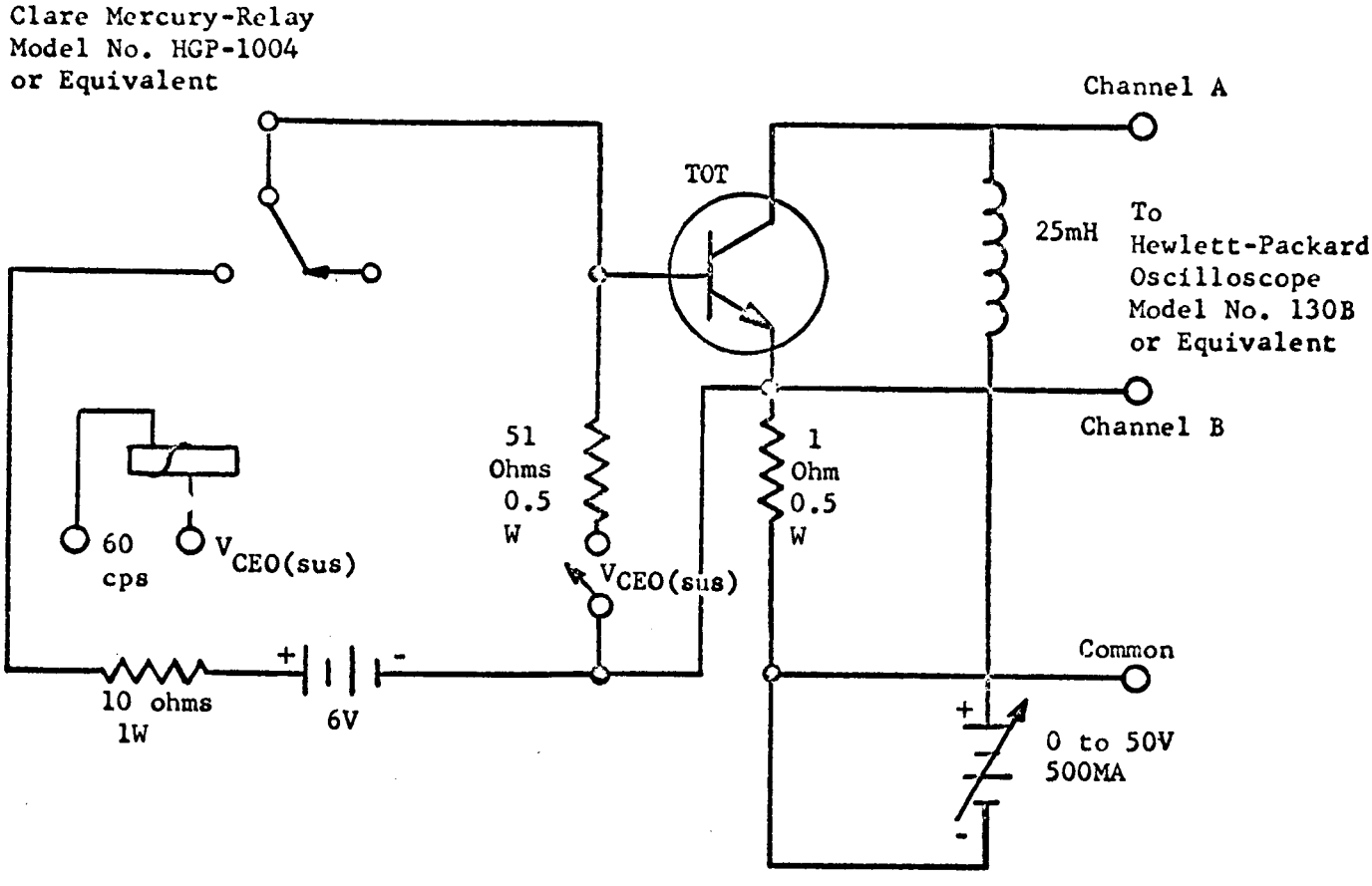


Figure 25: Sustaining Voltage Circuit

A type of rating which is coming into increased usage in the transistor industry is the so-called "maximum operating conditions." This rating method is valuable because it provides information concerning the ability of transistors to operate under pulsed conditions at high peak power levels, as well as under steady-state DC conditions.

At collector junction voltage levels much lower than the $V_{CEO(sus)}$ level and at moderate current levels, the power rating of a transistor may be determined simply from the maximum permissible junction temperature and the steady state or transient thermal impedance. However, at higher voltage and current levels, it is necessary to consider the effect of current crowding which may eventually lead to a mode of operation known as second breakdown. Although the second breakdown phenomenon is not completely understood, one cause is thought to be nonuniform biasing of the base-emitter junction, owing to lateral current flow in the base region. The resulting crowding of the collector current produces hot spots and the second-breakdown effect.

Second breakdown is characterized by an abrupt decrease in collector-emitter voltage to a low level, usually 20 volts or less. Operation in this mode for a period longer than several microseconds usually results in transistor degradation or failure. Although the term "second breakdown" is widely accepted, it has led to some confusion, since the phenomenon is not necessarily preceded by first (or avalance) breakdown.

Two general statements can be made about second breakdown:

1. It is always initiated from a region of relatively high dissipation on the collector characteristic family of curves.

2. There is a time lag before initiation, implying a temperature effect and a critical energy. This critical energy is affected by a number of factors: V_{CE}, case temperature, base-emitter bias and transistor design.

Two different types of maximum operating conditions are commonly specified each having usefulness in certain applications. The two types are differentiated by polarity of base-emitter bias.

1. Forward Bias

The maximum operating conditions for forward bias are defined by a V_{CE}, I_C, time relationship. This relationship is a pulse with a duration of 1, 2, 5 x 10^{-x} seconds. For each pulse width, a curve may be plotted on the collector family of curves (V_{CE} vs. I_C) which defines a "safe area" of operation, free from second breakdown. These curves are obtained from statistical, empirical data of critical second breakdown conditions.

The basic test circuit for obtaining the forward-biased data is shown in Figure 26. It should be noted that the value of the current sensing resistor, R_S, is sufficiently low that its voltage drop is negligible in comparison with V_{CC}. Forward bias for the pulse is supplied by the pulse generator. V_{BB} and R_{BB} are selected to provide reverse bias when the pulse generator is in the "off" condition. The load line for this test is shown in Figure 27. The general form of the "safe area" curves is shown in Figure 28.

2. Reverse Bias

The maximum operating conditions for reverse bias may be defined by an I_C vs. inductance relationship. This type of rating is based upon operation in an inductive load circuit because this is the only practical type of circuit in which appreciable amounts of energy are dissipated in a reverse-biased condition. The basic reverse-biased test circuit is given in Figure 29. The wave shapes are shown in Figure 30. The operation is as follows. The transistor is turned on by the pulse generator for a duration of time, t_1, which is sufficient to allow the collector current, I_C, to build up to a suitable value, I_1, in the inductance, L. The pulse generator

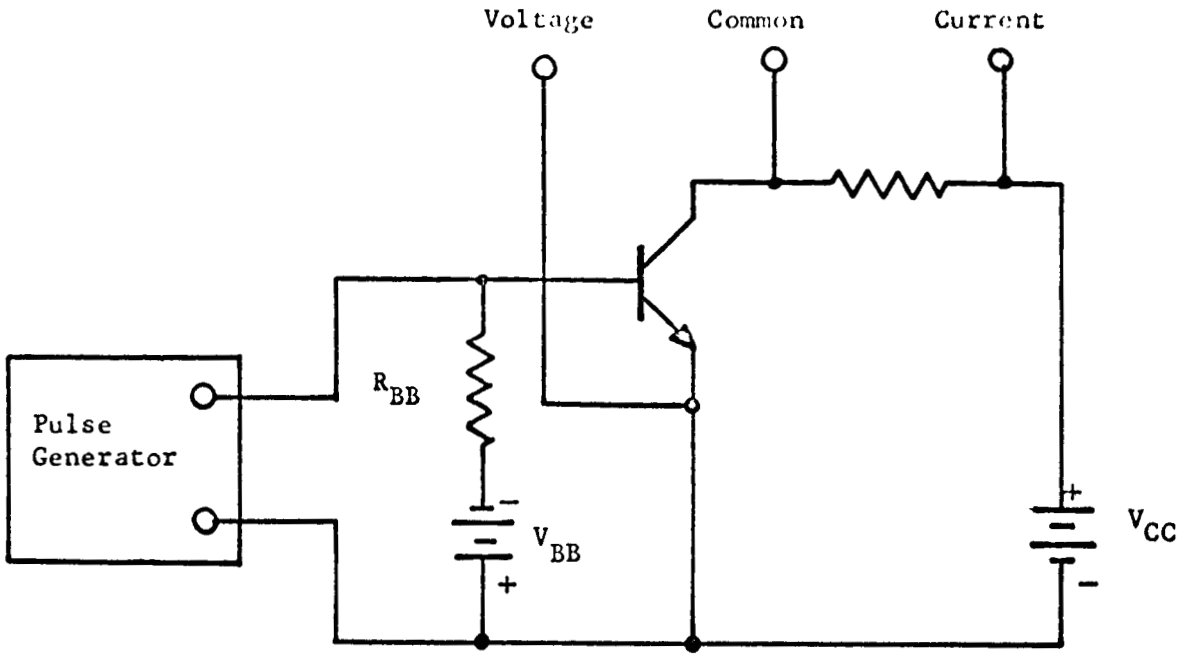


Figure 26: Forward Bias Peak Power Test Circuit

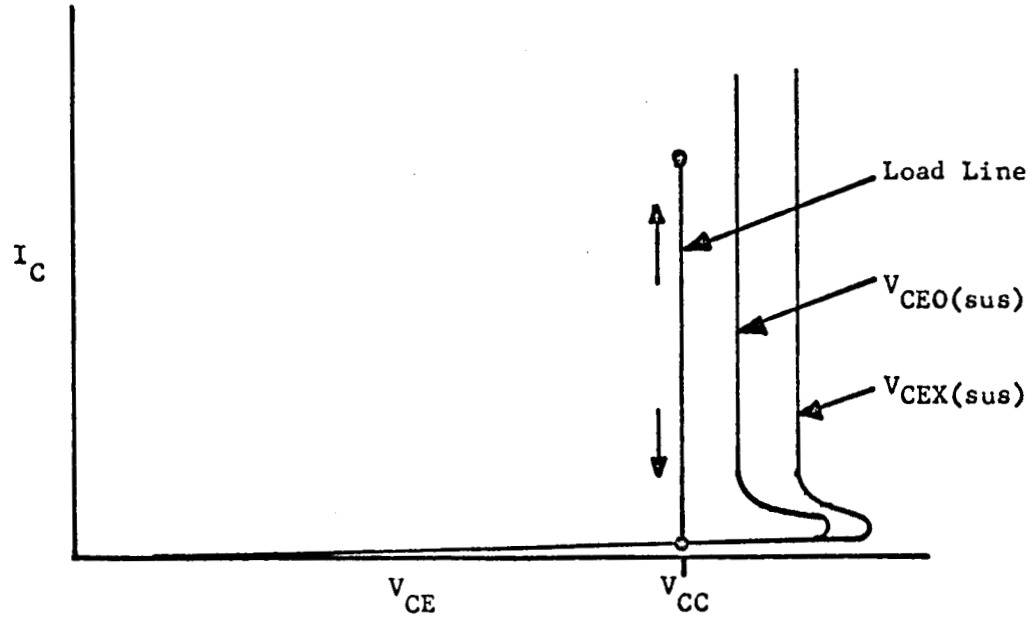


Figure 27: Load Line for Forward Bias Peak Power Test

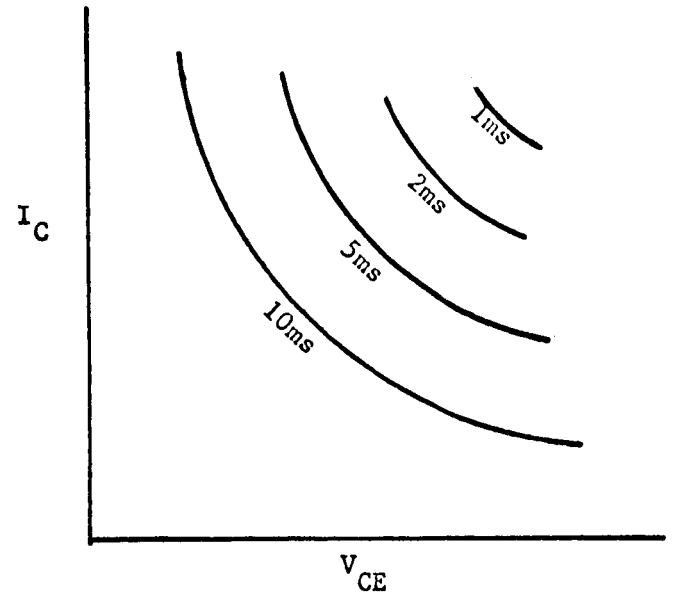


Figure 28: Forward Bias Maximum Operating Conditions

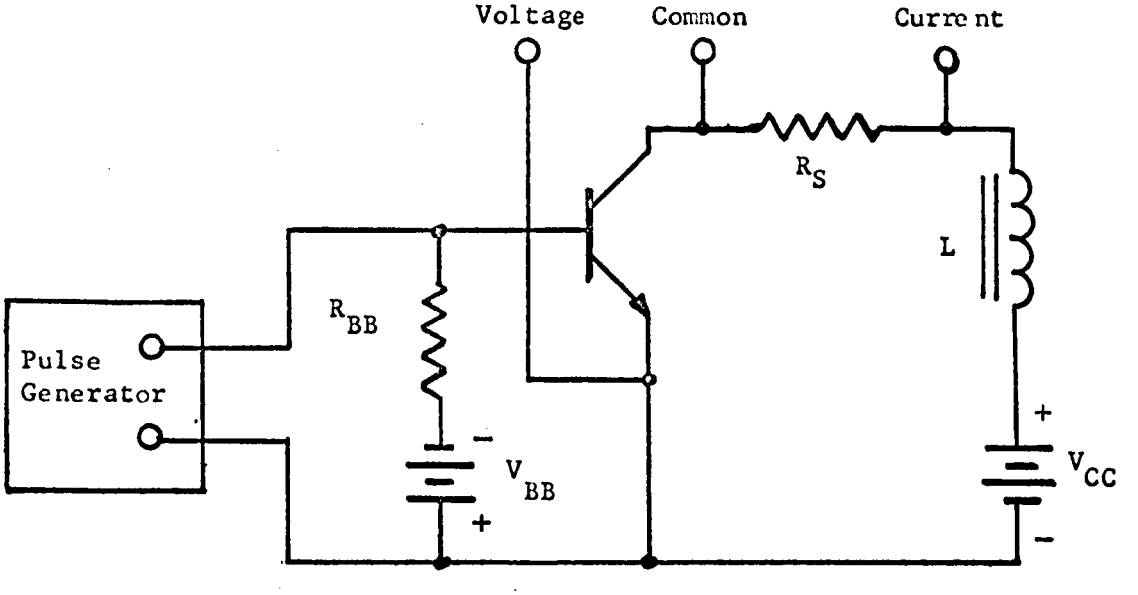


Figure 29: Reverse Bias Peak Power Test Circuit

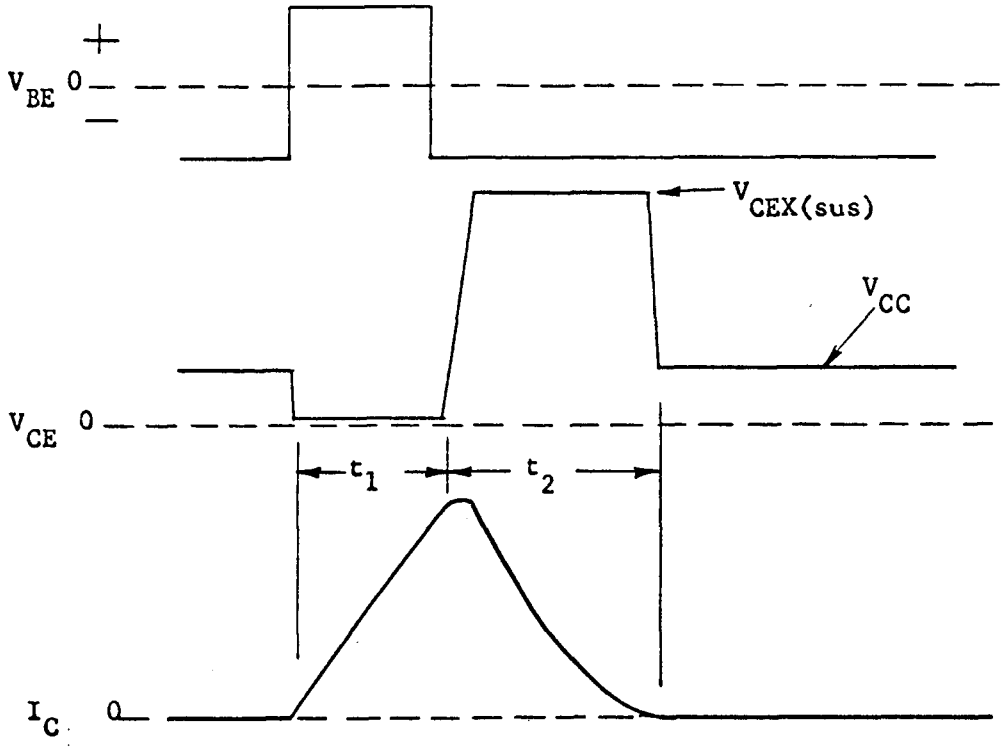


Figure 30: Reverse Bias Peak Power Test Wave Shapes

then turns off and the transistor is reverse-biased by supply V_{BB}. During the interval t_2, the transistor turns off, and the energy stored in the inductance is dissipated in the transistor. This energy is $1/2\ LI_1^2$. The load line for this test is shown in Figure 31. It should be noted that most of the energy is dissipated while the transistor's operating point is in the reverse-biased "sustaining region." As in the previous case, the resulting curves are drawn to exclude the critical conditions for second breakdown. The general form of the curves is shown in Figure 32.

In both forward- and reverse-bias testing, the objective is comparative evaluation of the transistors rather than the generation of applications oriented ratings. The tests are therefore performed at a very low duty cycle, such that the transistors return to thermal equlibrium with the ambient between power pulses. A case temperature of 25°C is used for convenience.

To permit nondestructive evaluation of second breakdown, a crowbar circuit turns off the test set as voltage begins to increase rapidly. Since the epi base transistors being studied are extremely fast, this circuit does not always afford absolute protection. Figure 33-a illustrates the waveform obtained when the transistor is in no danger of second breakdown. Figure 33-b shows the waveform as the transistor is beginning to go into second break. By stopping the test at this point, reproducible nondestructive results can be obtained.

A Dynatran, Model 2158, pulsed curve tracer is used for measurement of high current gain and $V_{CE(sat)}$. This equipment operates on approximately a 1% duty cycle with a collector pulse (triangular) of about 150μsec. The base supply is on about 300μsec. with the collector pulse centered in this time period. The unit is capable of 85 amps I_C at 4 volts V_{CE} and may also be

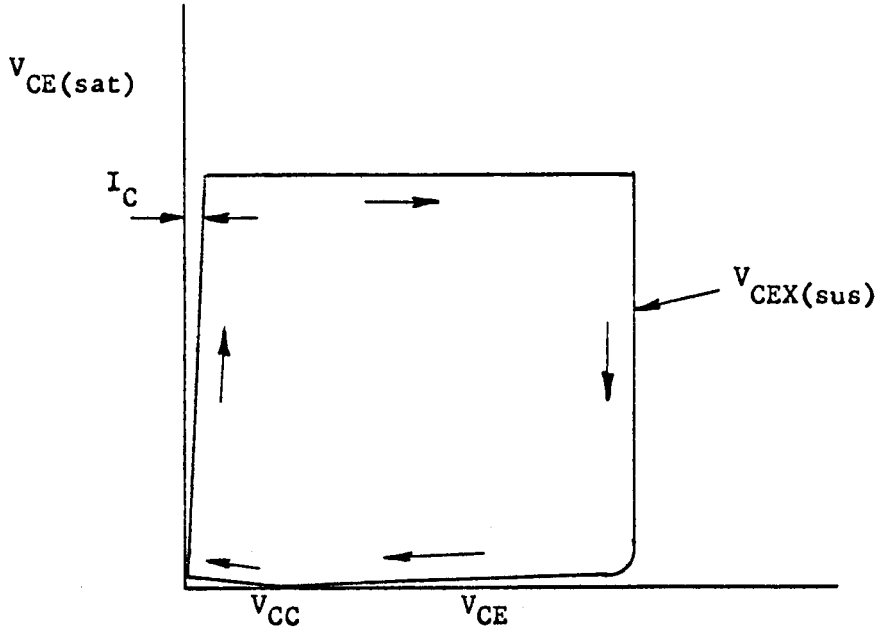


Figure 31: Reverse Bias Peak Power Test Load Line

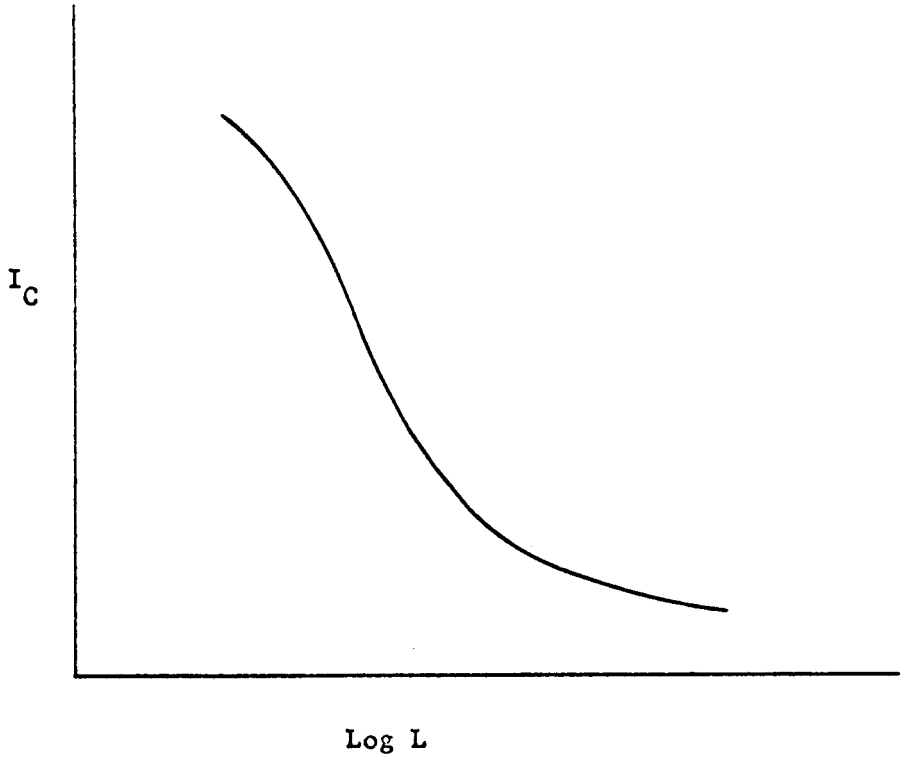


Figure 32: Reverse Bias Maximum Operating Conditions

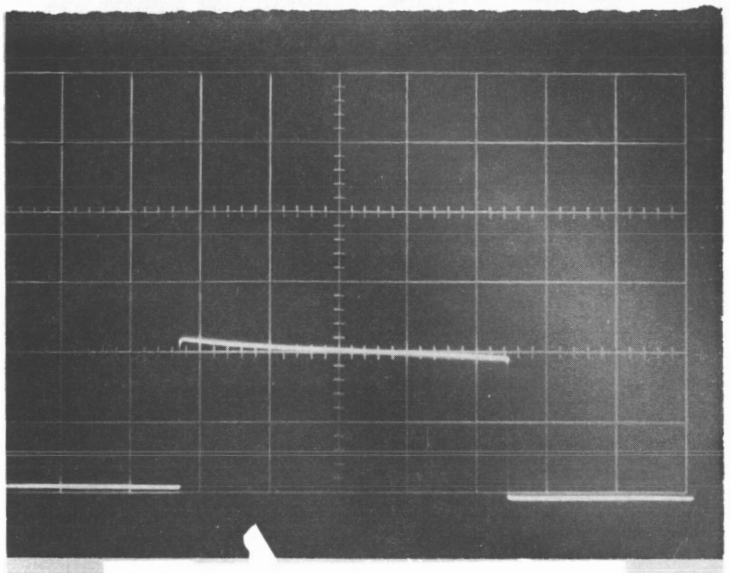


Figure 33-a

Vertical .5A/Div.

Horizontal 2.5ms/Div.

V_{CE} = 80V

Secondary Breakdown Waveforms

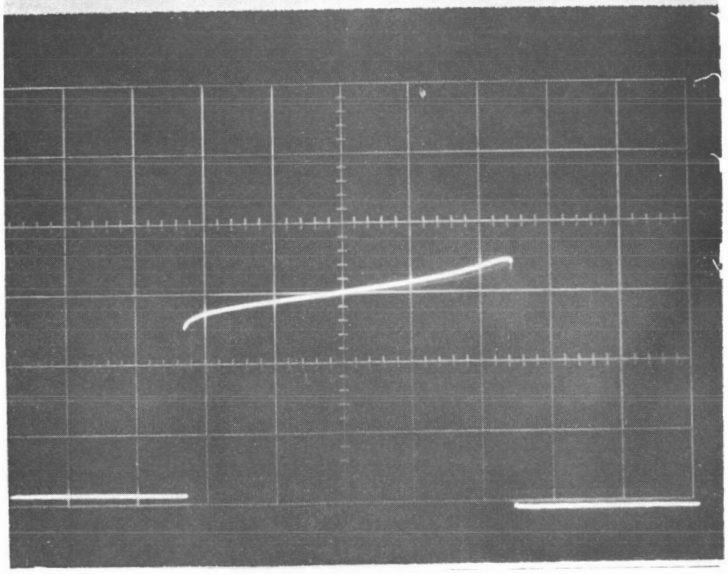


Figure 33-b

programmed for voltages up to 5000 volts with constant EI products. The collector characteristics are displayed on an integral oscilloscope for observing the collector sweep cycle. The base current is read off a peak reading voltmeter connected across a current shunt in series with the base circuit of the transistor under test. Base current ranges are available for 0 to 30 amps. Base-emitter (V_{BE}) voltage is also monitorable on either the integral oscilloscope or a second peak reading voltmeter connected through a voltage divider to the base and emitter terminals. All voltage measurements are made through independent probes to eliminate current lead resistance. Thus, we can successfully measure saturation voltages in the .1 volt range quite easily.

For testing the V_{CEX} leakage of these transistors, a 1.5 volt source is connected to the base and emitter of the transistor under test while sweeping the collector characteristics. The test is performed on approximately a 1% duty cycle to avoid high dissipations and heat sinking problems. Voltages and leakage currents are read off the integral oscilloscope in the Dynatran equipment. Frequency response is measured on a Westinghouse designed circuit.

The h_{fe} tester uses one-quarter wavelength transmission lines for isolation of the power supplies and also for the short circuit load. When a quarter wavelength of transmission line (cut to the selected frequency) is shorted on one end with a capacitor, the other end approaches an infinite input impedance. This high impedance end is connected to the transistor and the collector and base bias supplies are isolated from the RF. A quarter wavelength transmission line is connected to the collector-emitter terminals with a high impedance RF voltmeter connected to the other end of this transmission line. Since a quarter wavelength transmission line acts as an impedance transformer, the collector-emitter is essentially short-circuited to RF current. An input RF voltage is applied to the base and the base RF current is measured. The output RF current, using transmission line theory is $i_{out} = E_{out}/Z_o$ where E_{out} is the RF output current and Z_o is the

characteristic impedance of the transmission line. Therefore, $h_{fe} = i_o/i_{in}$ where i_o = output RF current and i_{in} = input RF current. The gain-bandwidth product f_t = frequency of measurement multiplied by h_{fe} when the frequency of measurements is on the 6db/octave slope.

A special switching time circuit has been design and constructed. It is shown schematically in Figure 34. An experimental Westinghouse 100-ampere single-diffused transistor has been used to demonstrate the capability of measuring switching at: I_B = 5A, I_C = 75A, V_{BB} = 1.5V and V_{CC} = 12V. A pulse generator with a 2 ampere peak and a 20 nanosecond rise time is used to drive Q_1 -- an experimental transistor with fast switching times. With Point A of Figure 34 returned to ground through a noninductive resistor, a 5-ampere peak pulse current was measured with less than 100 nanosecond rise and fall times.

The total switching time is the sum of the delay time (t_d), the rise time (t_r), the storage time (t_s) and the fall time (t_f) as shown in Figure 35.

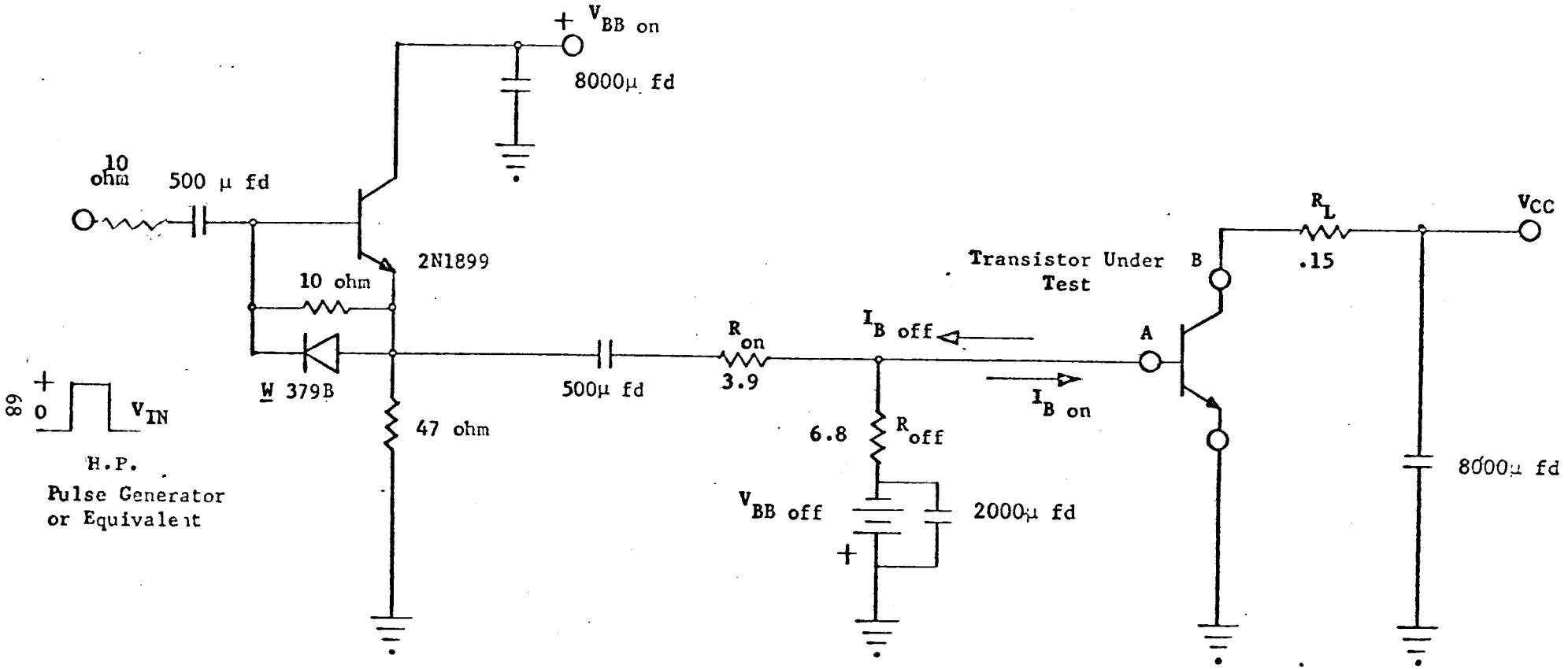
B. ELECTRICAL RESULTS

The initial phase of this study involved fabrication and evaluation of 30-ampere epi base transistors as an empirical method of optimizing the parameters for the 100-ampere transistors.

Tables II through VIII show the electrical results obtained for the three ranges of base widths for both the punch-through and avalanche conditions.

Figure 36 is a plot of maximum current (I_M) vs. the product of the base resistivity and the base width ($\rho_B W_B$). The maximum current is a measurement obtained by the previously described peak power test and is an indication of the relative strength of the transistor. Whereas the frequency response has a direct dependence on the base width, as shown by the graph, the peak power is affected by both base width and resistivity. Peak power is obviously improved by increasing base width and/or resistivity; however, the frequency requirement determines the upper limit on the base width. The resistivity of the base is determined by the breakdown voltage requirement. For the

SWITCHING TEST CIRCUIT FOR TRANSISTORS



I_B(ON) and I_B(OFF) measured at Point A
with Tektronix Type 131 Current Probe Amp.

I_C measured at Point B with Pearcon Electronics
Mod. 110 current transformer

TRANSISTOR TEST CONDITIONS

V_{CC} = 12V		Input Pulse
R_L = .15 ohm		cps rep.rat = 10 cps
I_C = 75A		μ sec pulse width = 100 sec
$I_{B\ on}$ = 5A		
R on = 3.9 ohm		
R off = 6.8 ohm		
V_{BB} on = 40V		
V_{BB} off = 1.5V		

Figure 34: Switching Time Circuit

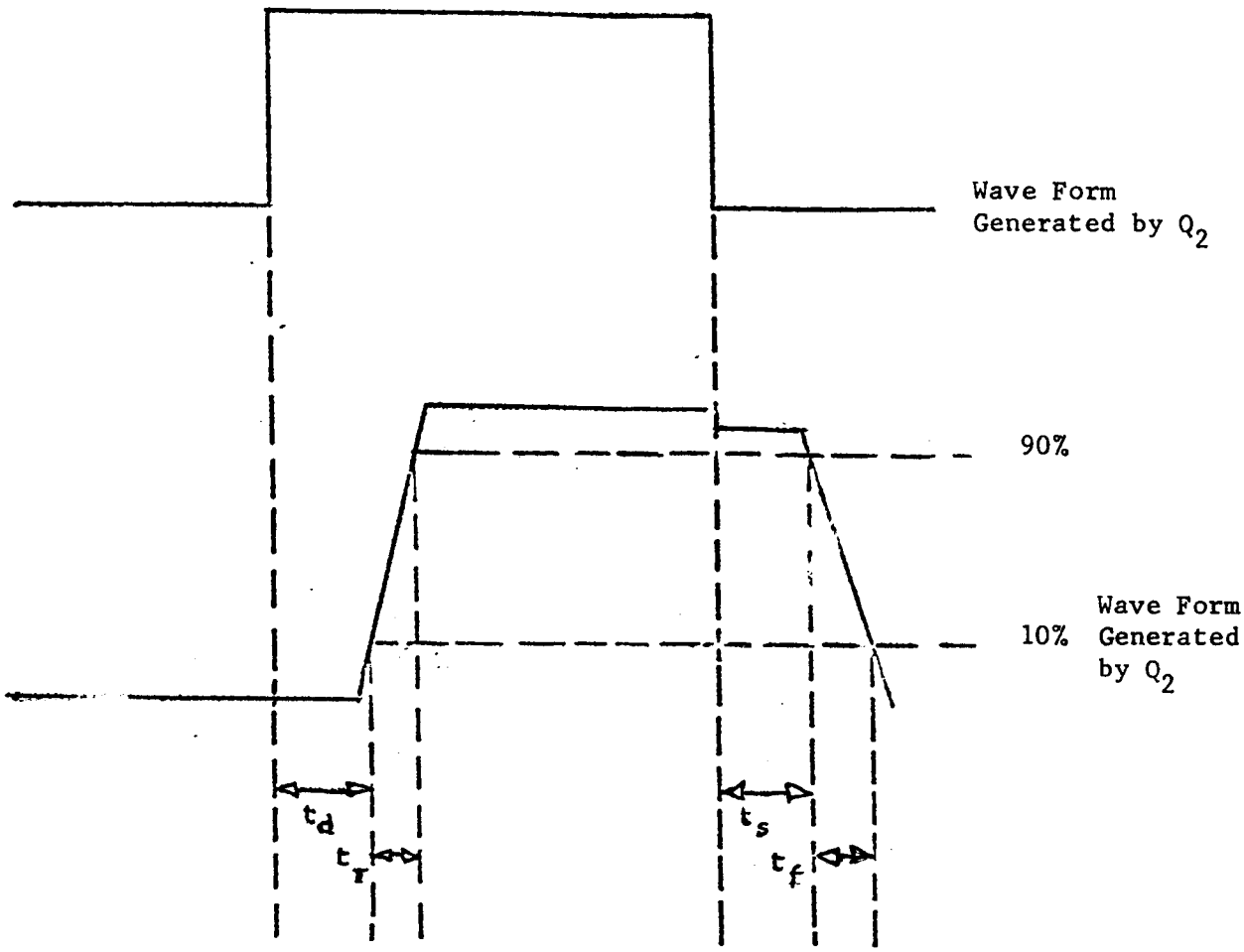


Figure 35: Switching Time Waveform

TABLE II

RUN NO. LR-1

30-Amp Transistor

Unit No.	V_{CBO} volts	I_{CBO} ma	V_{CEO} volts	I_{CEO} ma	V_{EBO} volts	I_{EBO} ma	h_{fe} 0.5A	h_{fe} 20A	V_{CE} sat. I_C=20A	V_{BE} sat.	f_t mc/s V_{CE}=10V I_C=3A	S/B V_{CE}=80V 10ms I_C, Amps	Sat. Switching V_{CC}=30V I_C=15A μsec.
1-1	150	.6	100	.8	5	.05	25	25	1.0	-	> 30	~ 1.0	1.0
1-2	150	12	100	20	5	.2	20	20	.8	-	> 30	~.9	1.0
1-3	150	4	100	6	5	1	25	20	1	-	> 30	~.85	1.0
1-4	150	.6	100	.8	5	.1	20	22	.9	-	> 30	~1.1	1.0

LR-1
Collector W = 20μ
Base x_j = 6.3μ
ρ = .5 ohm-cm
W_B = 2.7μ

TABLE III

RUN NO. NE-7

30-Amp Transistor

Unit No.	V_{CBO} volts	I_{CBO} ma	V_{CEO} volts	I_{CEO} ma	V_{EBO} volts	I_{EBO} ma	h_{fe} 0.5A	h_{fe} 20A	V_{CE} sat. I_C=20A	V_{BE} sat.	f_t mc/s V_{CE}=10V I_C=3A	S/B V_{CE}=80V 10ms I_C, Amps	Sat. Switching V_{CC}=30V I_C=15A µsec.
1-4	178	3	140	5	7.2	3.5	7.9	-	2.1	-	~15	.5	1.5 - 1.8
1-8	200	4	180	5	7.0	5	8.7	-	.82	-	~15	.5	1.5 - 1.8
3-10	150	7	110	10	7.2	.9	5.7	-	.6	-	~15	.6	1.5 - 1.8
3-8	150	8.5	130	10	7.0	.1	7.15	-	1.1	-	~15	.5	1.5 - 1.8
3-7	200	.7	200	.6	6.8	.015	7.3	-	.85	-	~15	1.0	1.5 - 1.8

NE-7

Collector W = 20µ

Base x_j = 11.1µ

ρ = .1 ohm-cm

W_B = 6.9µ

TABLE IV

RUN NO. NE-25

30-Amp Transistor

Unit No.	V_{CBO} volts	I_{CBO} ma	V_{CEO} volts	I_{CEO} ma	V_{EBO} volts	I_{EBO} ma	h_{fe} 0.5A	h_{fe} 20A	V_{CE} sat. I_C=20A	V_{BE} sat.	f_t mc/s V_{CE}=10V I_C=3A	S/B V_{CE}=80V 10ms I_C, Amps	Sat. Switching V_{CC}=30V I_C=15A µsec.
25-1	200	.02	200	.1	4	4	20	10	1	-	~15	1	1.5
25-2	200	.01	200	.01	4	5	30	15	1.2	-	~15	1.2	1.5
25-3	200	3	130	2	5	2	20	10	1.1	-	~15	1.1	1.6
25-4	180	2.5	140	5	4	2	30	14	1.3	-	~15	1.0	1.8
25-5	150	2.5	100	30	5	3	30	15	1.2	-	~15	1.2	1.5

NE-25

Collector W = 20µ

Base x_j = 11.7µ

ρ = 2.4 ohm-cm

W_B = 7.5µ

TABLE V

RUN NO. NE-30

30-Amp Transistor

Unit No.	V_{CBO} volts	I_{CBO} ma	V_{CEO} volts	I_{CEO} ma	V_{EBO} volts	I_{EBO} ma	h_{fe} 0.5A	h_{fe} 20A	V_{CE} sat. I_C=20A	V_{BE} sat.	f_t mc/s V_{CE}=10V I_C=3A	S/B V_{CE}=80V 10ms I_C, Amps	Sat. Switching V_{CC}=30V I_C=15A μsec.
1	150	4.5	95	10	14	5	11.2	10	2.0	2.55	9.1	> 1	1.5 - 1.8
2	150	2	150	2.5	5	40	16.2	16.6	1.2	1.65	9.5	.7	1.5 - 1.8
3	150	3.5	130	10	5	.2	11.2	13.3	2.0	2.55	9	> 1	1.5 - 1.8
4	150	6	80	10	5.5	5	22.2	10	1.5	2.0	13	.95	1.5 - 1.8
5	150	6	80	10	4.5	5	17	13.3	1.5	2.1	14.2	> 1	1.5 - 1.8
	250	.3	100	.2	25	.01	10	2.5	2.5	2.6	10	3.8	1.5 - 1.8

NE-30
Collector W = 16.8μ
Base x_j = 14.7μ
ρ = 1.0 ohm-cm
W_B = 10.8μ

TABLE VI

RUN NO. NE-33

30-Amp Transistor

Unit No.	V_{CBO} volts	I_{CBO} ma	V_{CEO} volts	I_{CEO} ma	V_{EBO} volts	I_{EBO} ma	h_{fe} 0.5A	h_{fe} 20A	V_{CE} sat. I_C=20A	V_{BE} sat.	f_t mc/s V_{CE}=10V I_C=3A	S/B V_{CE}=80V 10ms I_C, Amps	Sat. Switching V_{CC}=30V I_C=15A µsec.
1	150	.4	150	.3	5	1	2.1	1.1	1.3	2.1	1	> 1	-
2	150	.5	150	.5	5	10	1.7	1.7	1.5	2.3	1	> 1	-
4	150	.3	150	.3	4.5	2	1.7	1.7	1.2	2.15	1	> 1	-
5	150	.2	150	.2	5	4.5	1.4	1.4	2.0	2.9	1	> 1	-

NE-33

Collector W = 29.4µ

Base x_j = 18.3µ

ρ = .13 ohm-cm

W_B = 15.0µ

TABLE VII

RUN NO. NE-36

30-Amp Transistor

Unit No.	V_{CBO} volts	I_{CBO} ma	V_{CEO} volts	I_{CEO} ma	V_{EBO} volts	I_{EBO} ma	h_{fe} 0.5A	h_{fe} 20A	V_{CE} sat. I_C=20A	V_{BE} sat.	f_t mc/s V_{CE}=10V I_C=3A	S/B V_{CE}=80V 10ms I_C, Amps	Sat. Switching V_{CC}=30V I_C=15A µsec.
36-A-5	250	3	100	2.5	7.5	80	5	2.5	1.3	-	~ 2	4.6	~ 2.8
36-A-12	250	1	100	.01	10	6	2.1	1.9	1.9	-	~ 2	3.9	~ 2.8
36-A-18	150	.8	100	2.5	5	5	4	1.5	2.5	-	~ 2	3.4	~ 2.8
36-A-20	150	.4	100	.01	5	20	7	2	2.0	-	~ 2	4.1	~ 4.1

NE-36

Collector W = 21µ

Base x_j = 26.4µ

ρ = 5.9 ohm-cm

W_B = 18.3µ

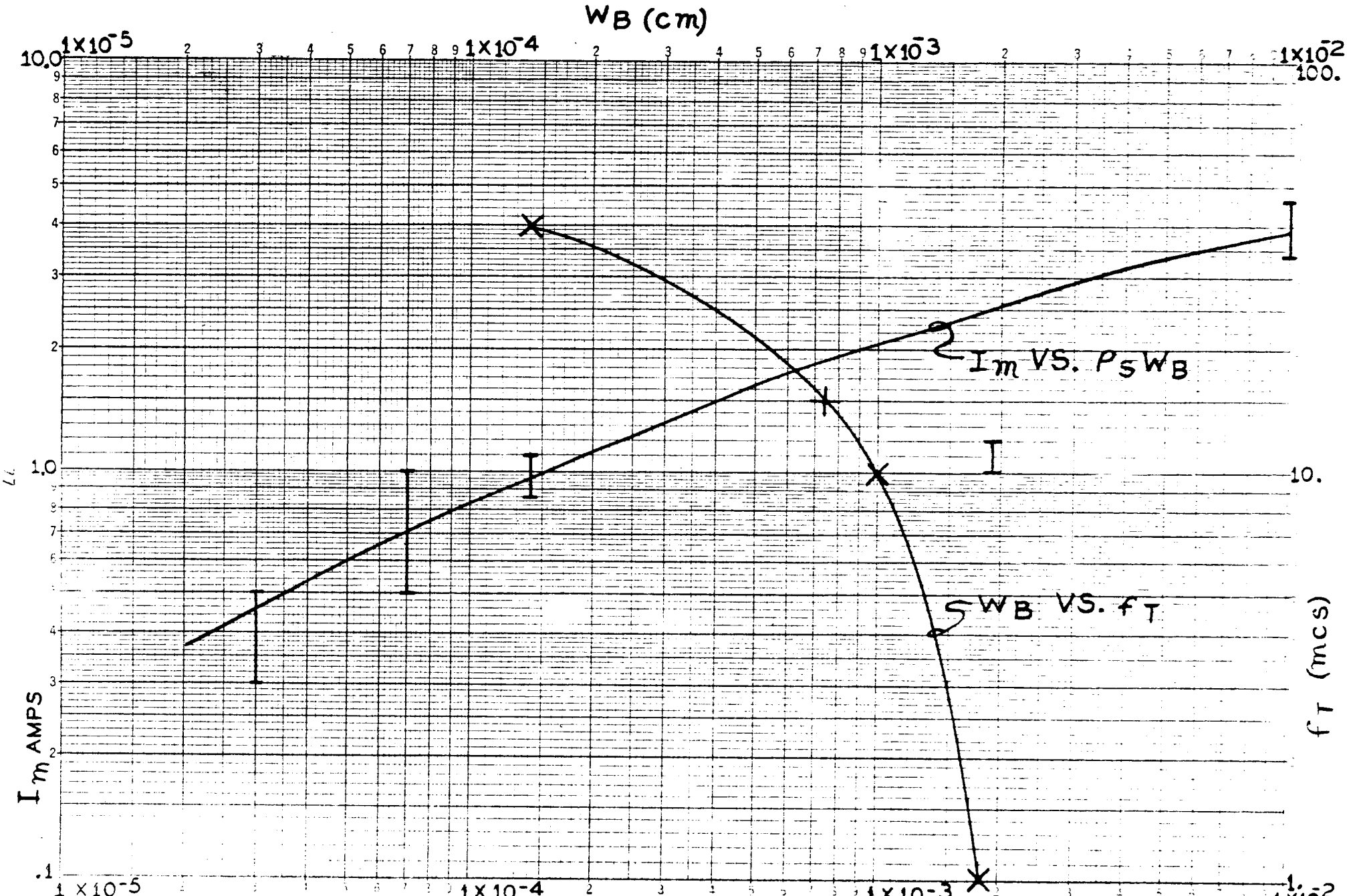
TABLE VIII

RUN NO. 54

30-Amp Transistor

Unit No.	V_{CBO} volts	I_{CBO} ma	V_{CEO} volts	I_{CEO} ma	V_{EBO} volts	I_{EBO} ma	h_{fe} 0.5A	h_{fe} 20A	V_{CE} sat. I_C=20A	V_{BE} sat.	f_t mc/s V_{CE}=10V I_C=3A	S/B V_{CE}=80V 10ms I_C, Amps	Sat. Switching V_{CC}=30V I_C=15A µsec.
54-85	150	3.5	150	3.5	5	.001	24.8	24.7	.85	1.05	> 30	.35	< 1.5
54-91	150	8.7	150	9	5	.7	30	28.6	.75	.92	> 30	.5	< 1.5
54-73	150	9	150	9	5	.035	27.8	25	1.95	2.4	> 30	.5	< 1.5
54-75	150	2.5	150	3.0	5	.065	33.4	30.8	.9	1.15	> 30	.5	< 1.5
54-81	150	1.4	150	2.0	5	.065	24.2	21.1	.9	1.4	> 30	.4	< 1.5
54-70	150	9.5	150	9.5	5	.001	34.1	30.4	.75	.95	> 30	1.1	< 1.5
54-79	150	1.5	150	.9	5	3.7	13	11.7	2.5	2.9	> 30	.3	< 1.5
54-64	150	5.5	150	13.0	5	.48	16.3	14.3	1.8	2.0	> 30	.5	< 1.5
54-94	150	.95	150	.9	5	.01	13.6	12.5	2.4	2.2	> 30	1.0	< 1.5

Collector	W_{54}	= 20µ
Base	x_j	= 6.3µ
	ρ	= .1 ohm-cm
	W_B	= 3.0µ



PEAK POWER CURVE FIG. 36

subject device to attain frequency cutoff in excess of 20mcs, the base width limit is $\sim 6\mu$.

In order to satisfy the breakdown and peak power requirements, as well as the switching speed requirement, the following conditions were employed for 100A sample fabrication:

ρ_B = 1.5-2.0 ohm-cm

W_B = 6-8μ .

Test results are given in Table IX.

Additional 100-ampere samples were fabricated using 3-5μ base widths and .5-.7 ohm-cm base resistivity. As expected, the switching speeds are faster but the voltage is somewhat reduced. The electrical results of these samples are given in Table X.

In both cases, a modification of collector resistivity was required to reduce the saturation voltage of the final samples. The electrical results of the initial 100-ampere wafers with $\sim$50 ohm-cm epitaxial collector is given in Table XI. The resistivity of the epitaxial collector was reduced to $\sim$10 ohm-cm, thereby reducing the saturation voltages accordingly.

Table IX: Wide W_B 100-Amp Samples - Electrical Parameters

NAS8-18125

Unit No.	V_{CBO} volts	I_{CBO} ma	V_{CEX} volts	I_{CEX} ma	V_{EBO} volts	I_{EBO} ma	h_{FE} I_C=.5A V_{CE}=3V	h_{FE} I_C=60A V_{CE}=4V	h_{FE} I_C=100A V_{CE}=4V	$V_{CE(sat)}$ I_C=75A I_B=7.5A or 1 1/2 I_B	$V_{CE(sat)}$ I_C=100A I_B=10A or 1 1/2 I_B	$V_{BE(sat)}$ I_C=100A I_B=10A or 1 1/2 I_B
NE-66-2	80	.2	150	.2	1.5	.2	7	6	--	1.5	1.8	2.5*
NE-71-4	80	1	150	2	1.5	3	20	20	23	.5	1.5	2.18*
NE-77-6	80	.3	150	1.5	1.5	3	25	35	20	.35	.4	1.5+
NE-80	80	.15	150	1	1.5	5	30	80	50	.19	.2	1.25+
NE-82-1	80	2	150	8	1.5	70	10	30	22	.45	.7	1.65+
NE-82-2	80	.5	150	4	1.5	8	12	25	16	.5	.5	1.7+
NE-83-1	80	3	150	20	1.5	7	20	55	33	.25	.4	1.9+
NE-83-2	80	.5	150	1.2	1.5	8	25	35	20	.4	.6	1.8+
NE-83-3	80	.6	150	1.5	1.5	4	16	35	21	.4	.45	1.7+
NE-83-4	80	.1	150	.4	1.5	6	15	25	16	.5	.6	1.7+

* Base resistivity = 1.5-2.0 ohm-cm, W_B = 6-8μ; Collector resistivity > 50 ohm-cm.
\+ Base resistivity = 1.5-2.0 ohm-cm, W_B = 6-8μ; Collector resistivity = 25 ohm-cm.

Saturated Switching at V_{CC} = 12V; I_B = 5A

Unit No.	I_C amp	$t_d + t_r$ μsec.	t_s μsec.	t_f μsec.	t_{tot} μsec.
NE-82-1	50*	2.1	1.3	1.8	5.2
NE-82-2	50*	2.0	1.0	1.4	4.4
NE-83-2	50*	2.3	2.2	1.4	6.0
NE-83-4	50*	3.0	.4	2.4	5.8
NE-80	75	4.7	1.8	3.0	9.5
NE-82-1	75	3.5	1.0	1.8	6.3
NE-83-1	75	3.7	1.4	2.5	7.6
NE-83-3	75	3.2	1.0	1.5	5.7

* Forced gain = 10

Table X: Narrow W_B 100-Amp Samples - Electrical Parameters

NAS8-18125

Unit No.	V_{CBO} volts	I_{CBO} ma	V_{CEX} volts	I_{CEX} ma	V_{EBO} volts	I_{EBO} ma	h_{FE} I_C=.5A V_{CE}=3V	h_{FE} I_C=60A V_{CE}=4V	h_{FE} I_C=100A V_{CE}=4V	$V_{CE(sat)}$ I_C=75A I_B=10.0A or 1 1/2 I_B	$V_{BE(sat)}$ I_C=75A I_B=10A or 1 1/2 I_B	$V_{BE(sat)}$ I_C=100A I_B=10A or 1 1/2 I_B
NE-72	80	2	120	150	1.5	1	25	60	40	.6		2.3*
NE-96	80	60	100	100	1.5	100	12	30	--	.52	1.3	-- +
NE-96-1	80	20	100	25	1.5	200	15	30	--	.52	1.3	-- +
NE-97	80	6	100	10	1.5	6	15	20	--	.6	1.4	-- +
NE-98	80	2	100	2	1.5	30	12	16	--	.6	.9	-- +

* Base resistivity = .5-.7 ohm-cm, W_B = 3-5μ; Collector resistivity > 50 ohm-cm.

\+ Base resistivity = .5-.7 ohm-cm, W_B = 3-5μ; Collector resistivity = 25 ohm-cm.

Saturated Switching at V_{CC} = 12V; I_B = 5A

Unit No.	I_C amp	$t_d + t_r$ μsec.	t_s μsec.	t_f μsec.	t_{tot} μsec.
NE-96	>50	2.8	.8	2.1	5.7
NE-96-1	> 5	4.2	.5	2.5	7.2
NE-97	> 5	2	.5	1.5	4.0
NE-98	> 5	2.3	.5	1.6	4.4

TABLE XI

100 AMPERE TRANSISTORS, ELECTRICAL PARAMETERS

(Pre-Lid Weld)

Unit No.	V_{CBO} I_{CBO}	V_{CEO} I_{CEO}	V_{EBO} I_{EBO}	h_{FE} .5A	h_{FE} 75A 4V	h_{FE} 100A 4V	V_{CE} sat 75A	V_{CE} sat 100A	V_{CEO} (sus) at 200ma
NE-66-1	250V 25ma	200V 40ma	4V	5	10	9	1.5V	2V	200V
NE-71-1	250V .4ma	225V .2ma	5V 3.5ma	12.0	-	20	-	1.25	200V
NE-60-3	105V 10ma	105V 10ma	4V 160ma	6	9	5	1.5V	-	-
NE-75-1	150/10 200/25	100/14 150/40	5/.8	-	18	16	1.5V	2.2	-

> 50 ohm-cm collector resistivity

VII. SUMMARY AND RECOMMENDATIONS

On a previous contract, NAS8-5335, a large area (22mm diameter), single unit, high power (150V x 100A), high speed (4μs) transistor was developed using a multiple epitaxial structure. In the present contract, the reliability performance, that is, secondary breakdown under peak power operation, was related to the design parameters. In addition, means to correlate device quality with material perfection and process control were established by using nondestructive X-ray diffraction techniques. Although it is beyond the scope of the present contract to fully apply these techniques in the first generation devices, it is strongly recommended that the basic design, the new processes, the material and evaluation techniques should be integrated and applied to the establishment of a transistor technology with built-in reliability potential.

For large area devices, the need for stringent control, reproducibility and material and process evaluation are obvious. In view of problems such as "pipes," high temperature processing strains, crystal inclusions, etc., the successful implementation of the recommended development should advance the semiconductor technology to a new level of performance and reliability.